Freescale Semiconductor
Addendum

Document Number: MPC8260UMAD
Rev. 2.4, 12/2011

Errata to the MPC8260 PowerQUICC II Family Reference Manual, Rev. 2

This errata document describes corrections to the *MPC8260 PowerQUICC II Family Reference Manual*, Revision 2. For convenience, the section number and page number of the errata item in the reference manual are provided. Items with section and page numbers in bold are new since the last revision of this document.

To locate any published updates for this document, see the website located on the last page of this document.

Section, Page No.	Changes
2.4.2.3, 2-20	Replace information regarding AN1767 with AN2129, as follows: "*Instruction and Data Cache Locking on the e300 Processor Core* application note (order number: AN2129)."
4.3.1.1, 4-18	In Table 4-4, "SICR Field Descriptions," add the following sentence to the field description of HP (bits 2–7): "Port C interrupts have a fixed priority level and cannot be advanced to the highest priority level."
4.3.1.4, 4-21	In Figure 4-14, change the lower bits at address 0x10C10 to be 0x10C0A.
4.3.2.13, 4-43	The L_TESCR2[PB] bits are incorrectly shown as shown as bits 12-15. Changed Figure 4-34 and Table 4-18 to show PB field as bits 8-11. Bits 0–7 and bits 12–15 are reserved and should be cleared, as shown below.

0–7	—	Reserved, should be cleared.
8–11	PB	Parity error on byte. There are four parity error status bits, one per 8-bit lane. A bit is set for the byte that had a parity error.
12–15	—	Reserved, should be cleared.

9.6, 9-4	Changed the referenced default value of ALRH to 0x0126_3457.
9.11.1.6, 9-33	Changed the description to clarify that the preload timer value description should reference the CPM clock.

23–0	Preload timer value	Preload value for 24-bit discard timer. Delayed PCI read transactions to a non-prefetchable address space remain valid within the PCI bridge a minimum of (224 – Preload Timer Value) internal CPM clock cycles. The discard timer is used to discard delayed reads from non-prefetchable address space if the master has not repeated the transaction in n internal CPM clock cycles, where n = (2^{24} - Preload Timer Value). Valid Preload Timer Values are in the range 0x000000–0xFFFFFE. Example: To discard a delayed completion if the PCI master has not repeated the transaction in 2^{15} PCI clocks and the internal frequency is 2 to 1 to the PCI bus. The Preload Timer Value should equal $2^{24} – 2^{16}$ (0xFF0000).

10.8, 10-9	In Table 10-2, modify the description for bit 29, SCCR[CLPD], to read: 1 CPM and SIU enter low power mode when the core does.
11.1, 11-3	Remove the words "for single accesses" from the end of the bulleted item which reads "Read-modify-write (RMW) odd/even parity..."
11.2.4, 11-8	Add the following first paragraph: RMW parity mode is used when there is a special memory byte lane for parity with its own byte enable, and actual RMW transaction would occur only for sub-port size write transaction. Normal parity mode is used when each data byte lane is appended with a parity bit, using the same byte enable.
11.4.6.4, 11-41	Replaced the last sentence of the section with the following: The most efficient programming will be CL – 1, but in some cases this setting can violate tRAS (activate to precharge) for a single beat read. If this happens, LDOTOPRE should be set to the minimum that meets tRAS.

Section, Page No.	Changes
18.8.5, 19-24	In Table 20-6, “IDMA BD Field Descriptions,” revise the description for bit 15, DDTB, as follows: 01 The destination address lies within the local or PCI buses.
20.1.4, 20-10	In Table 20-3, “TODR Field Descriptions,” in TOD field description, change “TOD is cleared automatically after one serial clock...” to say “TOD is cleared automatically after 1 system clock...”
20.3.2, 20-15	In Table 20-6, “RFCRx/TFCRx Field Descriptions,” revise the description for bits 3–4, RFCR/TFCR[BO], as follows: Byte ordering. This bit field should be set by the user to select the required byte ordering for the data buffer. If this bit field is modified on the fly, it will take effect at the beginning of the next frame. 00 Reserved. 01 PowerPC™ little-endian, or munged, byte ordering. As data is transmitted onto the serial line from the data buffer, the least significant byte of the buffer double word contains data to be transmitted earlier than the most-significant byte of the same buffer double word. 1X PowerPC byte ordering—normal operation. It is also called big-endian byte ordering. As data is transmitted onto the serial line from the data buffer, the most significant byte of the buffer word contains data to be transmitted earlier than the least significant byte of the same buffer word.
24.8, 24-7	In Table 24-5, change the third sentence in the Transmitter Underrun description to read as follows: Underrun in transparent mode occurs when the CPM or SDMA is experiencing a latency issue and cannot keep up with the transmission rate.
27.2.3.1, 27-8	In Table 27-3, “RFCRx/TFCRx Field Descriptions,” revise the description for bits 3–4, RFCR/TFCR[BO], as follows: Byte ordering. This bit field should be set by the user to select the required byte ordering for the data buffer. If this bit field is modified on the fly, it will take effect at the beginning of the next frame. 00 DEC (and Intel) convention is used for byte ordering—swapped operation. It is also called little-endian byte ordering. The transmission order of bytes within a buffer word is reversed as compared to the PowerPC mode. This mode is supported only for 32-bit port size memory. 01 PowerPC little-endian, or munged, byte ordering. As data is transmitted onto the serial line from the data buffer, the least significant byte of the buffer double word contains data to be transmitted earlier than the most significant byte of the same buffer double word. 1X PowerPC byte ordering—normal operation. It is also called big-endian byte ordering. As data is transmitted onto the serial line from the data buffer, the most significant byte of the buffer word contains data to be transmitted earlier than the least significant byte of the same buffer word.

Section, Page No.	Changes
28.9.2, 28-46	In Table 28-23, “TxBD Field Descriptions,” for bit 4, “L,” add the following note to the field description: **Note:** In Transparent Mode operation, setting Last puts the channel to Idle state after sending the last byte of the buffer (or the CRC, if enabled). To resume transmit, set the POL bit in the CHAMR. For continuous transmission—for example, with no concept of a frame boundary—Last should NOT be set in Transparent Mode.
29.10.1.1	Modify Section 29.10.1.1, “Re-Initialization Procedure,” as follows: 1.Disable the FCC transmission by clearing GFMR[ENT]. 2.Remember the TxBD pointer range for data recovery (Every TxBD marked Ready contains data that has not been transmitted). Clear the Ready bit of the entire TxBD ring. 3.Issue an “INIT TX PARAMS” command using the CPCR. 4.Enable FCC transmission by setting GFMR[ENT] and poll TSTATE[8:31] until it is cleared. 5.Issue a “Graceful Tx Stop” command using CPCR 6.Restore the Ready bit for all TxBDs marked for data recovery. 7.Modify TBPTR in PRAM to point to the TxBD to be transmitted next. 8.Issue a “Restart Tx” command using the CPCR.
29.10.1.3	Remove section, “Adjusting Transmitter BD Handling.”
30.10.2.3.2, 30-56	In Table 30-23, change the second sentence of the field description for TCT[SN] to read “Used to generate the sequence number in the AAL1 PDU header.”
35.7, 35-8	Remove paragraph with references to FPSMR[ECM].
35.8, 35-11	In Table 35-2, change description for location 0xFC to “**Reserved and must be cleared**,” in bold font.
35.19, 35-23	In Figure 35-8, “Fast Ethernet Receive Buffer (RxBD),” and Table 35-10, “RxBD Field Descriptions,” remove references to RxBD[CMR]. Bit 6 should be reserved.
38.5.1, 38-12	In Table 38-6, “RFCRx/TFCRx Field Descriptions,” revise the description for bits 3–4, RFCR/TFCR[BO], as follows: Byte ordering. This bit field should be set by the user to select the required byte ordering for the data buffer. If this bit field is modified on the fly, it will take effect at the beginning of the next frame. 00 DEC (and Intel) convention is used for byte ordering—swapped operation. It is also called little-endian byte ordering. The transmission order of bytes within a buffer word is reversed as compared to the PowerPC mode. This mode is supported only for 32-bit port size memory. 01 PowerPC little-endian, or munged, byte ordering. As data is transmitted onto the serial line from the data buffer, the least significant byte of the buffer double word contains data to be transmitted earlier than the most significant byte of the same buffer double word.

1X PowerPC byte ordering—normal operation. It is also called big-endian byte ordering. As data is transmitted onto the serial line from the data buffer, the most significant byte of the buffer word contains data to be transmitted earlier than the least significant byte of the same buffer word.

39.5, 39-10 In Table 39-7, “RFCR/TFCR Field Descriptions,” modify the second encoding in GBL (bit 2) field description to be for “1,” not “0.”

39.5, 39-11 In Table 39-7, “RFCRx/TFCRx Field Descriptions,” revise the description for bits 3–4, RFCR/TFCR[BO], as follows:

Byte ordering. This bit field should be set by the user to select the required byte ordering for the data buffer. If this bit field is modified on the fly, it will take effect at the beginning of the next frame.

00 DEC (and Intel) convention is used for byte ordering—swapped operation. It is also called little-endian byte ordering. The transmission order of bytes within a buffer word is reversed as compared to the PowerPC mode. This mode is supported only for 32-bit port size memory.

01 PowerPC little-endian, or munged, byte ordering. As data is transmitted onto the serial line from the data buffer, the least significant byte of the buffer double word contains data to be transmitted earlier than the most significant byte of the same buffer double word.

1X PowerPC byte ordering—normal operation. It is also called big-endian byte ordering. As data is transmitted onto the serial line from the data buffer, the most significant byte of the buffer word contains data to be transmitted earlier than the least significant byte of the same buffer word.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

Document Number: MPC8260UMAD
Rev. 2.4
12/2011