CY8CMBR2110

CapSense® Express™ 10-Button Controller

Features

- Register-configurable CapSense® controller
  - Does not require firmware or device programming
  - Ten-button solution configurable through I^2C protocol
  - Ten general purpose outputs (GPOs)
  - GPOs are linked to CapSense buttons
  - GPOs support direct LED drive
- SmartSense™ Auto-Tuning
  - Maintains optimal button performance even in noisy environment
  - CapSense parameters dynamically set in runtime
  - Saves time and effort in device tuning
  - Wide parasitic capacitance (C_P) range (5 pF–40 pF)
- Advanced features
  - Robust sensing even with closely-spaced buttons – Flanking Sensor Suppression (FSS)
  - User-configurable LED effects
    - On-system power-on
    - On-button touch
    - LED ON Time after button release
    - Standby Mode LED Brightness
  - Buzzer Signal Output
  - Supports analog voltage output (requires external resistors)
  - Attention line interrupt to host to indicate any CapSense button status change
  - CapSense performance data through I^2C interface
  - Simplifies production-line testing and system debug
- Noise Immunity
  - Specifically designed for superior noise immunity to external radiated and conducted noise
  - Low radiated noise emission
- System diagnostics of CapSense buttons – reports faults at device power-up
  - Button shorts
  - Improper value of modulating capacitor (C_{MOD})
  - Parasitic capacitance (C_P) value out of range
- EZ-Click™ Customizer tool
  - Simple graphical configuration options
  - Dynamically configures all features
  - Configurations can be saved and reused later
- I^2C interface
  - No clock stretching
  - Supports speed of up to 100 kHz
- Wide operating voltage range
  - 1.71 V to 5.5 V – ideal for both regulated and unregulated battery applications
- Low power consumption
  - Supply current in run mode as low as 23 µA[1] for each button
  - Deep sleep current: 100 nA
- Industrial temperature range: –40 °C to +85 °C
- 32-pin Quad Flat No-leads (QFN) package (5 mm × 5 mm × 0.6 mm)

Overview

The CY8CMBR2110 CapSense Express™ capacitive touch sensing controller saves time and money, quickly enabling a capacitive touch sensing user interface in your design. It is a register-configurable device and does not require any firmware coding or device programming. In addition, this device is enabled with Cypress's SmartSense Auto-Tuning algorithm which eliminates the need to manually tune the user interface during development and production ramp. This speeds the time to volume and saves valuable engineering time, test time, and production yield loss.

The EZ-Click Customizer tool is a simple graphical interface for configuring the device features, through the I^2C interface. One configuration can be used to configure multiple samples in different boards.

The CY8CMBR2110 CapSense controller supports up to ten capacitive sensing buttons and ten GPOs. The GPO is an active low output controlled directly by the CapSense input making it ideal for a wide variety of consumer, industrial, and medical applications. The wide operating range of 1.71 V to 5.5 V enables unregulated battery operation, further saving component cost. The same device can also be used in different applications with varying power supplies.

This device supports ultra low-power consumption in both run mode and deep sleep modes to stretch battery life. In addition, this device also supports many advanced features, which enhance the robustness and user experience of the end solution. The key advanced features are Noise Immunity and Flanking Sensor Suppression (FSS). Noise Immunity improves the immunity of the device against radiated and conducted noise, such as audio and radio frequency (RF) noise. FSS provides robust sensing even with closely-spaced buttons. FSS is a critical requirement in small form-factor applications.

Power-on LED effects provide visual feedback to the design at system power-on. Button-controlled LED effects provide visual feedback on a button touch. These effects improve the aesthetic value of the end product. Buzzer Signal Output provides audio feedback on a button touch. System diagnostics test for design faults at power-on and report any failures. This simplifies production-line testing and reduces manufacturing costs. CapSense data output through I^2C gives critical information about the design, such as button C_P and signal-to-noise ratio (SNR). This further helps in system debug and production-line testing.

Note

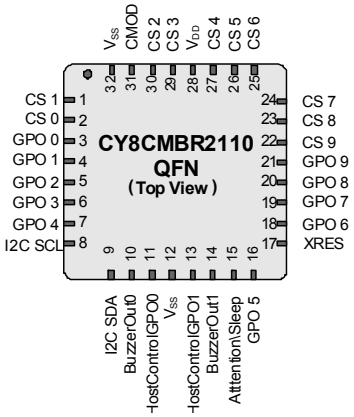
1. 23 µA per button (4 buttons used, 180 button touch per hour, average button touch time of 1000 ms, buzzer disabled, Button Touch LED Effects disabled, 10 pF < C_P of all buttons < 20 pF, Button Scan Rate = 541 ms, with power consumption optimized, Noise Immunity level Normal, CSx sensitivity Medium).

Contents

Pinout

Table 1. Pin Diagram and Definitions – CY8CMBR2110

Pin	Label	Type [2]	Description	If Unused
1	CS1	AI	CapSense button input, controls GPO1	Ground
2	CS0	AI	CapSense button input, controls GPO0	Ground
3	GPO0	DO	GPO activated by CS0	Leave open
4	GPO1	DO	GPO activated by CS1	Leave open
5	GPO2	DO	GPO activated by CS2	Leave open
6	GPO3	DO	GPO activated by CS3	Leave open
7	GPO4	DO	GPO activated by CS4	Leave open
8	I2C SCL	DIO	I^2C Clock line	N/A
9	I2C SDA	DIO	I^2C Data line	N/A
10	BuzzerOut0	DO	Buzzer output pin 0/GPO controlled by register settings	Leave open
11	HostControlGPO0	DO	GPO controlled by Register settings	Leave open
12	V_{SS}	P	Ground	N/A
13	HostControlGPO1	DO	GPO controlled by Register settings	Leave open
14	BuzzerOut1	DO	Buzzer output pin 1/GPO controlled by register settings	Leave open
15	Attention/Sleep	DIO	Used to control I^2C communication, device power consumption, and device operating mode	V_{DD}
16	GPO5	DO	GPO activated by CS5	Leave open
17	XRES	DI	Device reset, active high, with internal pull down	Leave open
18	GPO6	DO	GPO activated by CS6	Leave open
19	GPO7	DO	GPO activated by CS7	Leave open
20	GPO8	DO	GPO activated by CS8	Leave open
21	GPO9	DO	GPO activated by CS9	Leave open
22	CS9	AI	CapSense button input, controls GPO9	Ground
23	CS8	AI	CapSense button input, controls GPO8	Ground
24	CS7	AI	CapSense button input, controls GPO7	Ground
25	CS6	AI	CapSense button input, controls GPO6	Ground
26	CS5	AI	CapSense button input, controls GPO5	Ground
27	CS4	AI	CapSense button input, controls GPO4	Ground
28	V_{DD}	P	Power	N/A
29	CS3	AI	CapSense button input, controls GPO3	Ground
30	CS2	AI	CapSense button input, controls GPO2	Ground
31	C_{MOD}	AI	External modulating capacitor, recommended value 2.2 nF (±10%)	N/A
32	V_{SS}	P	Ground	N/A

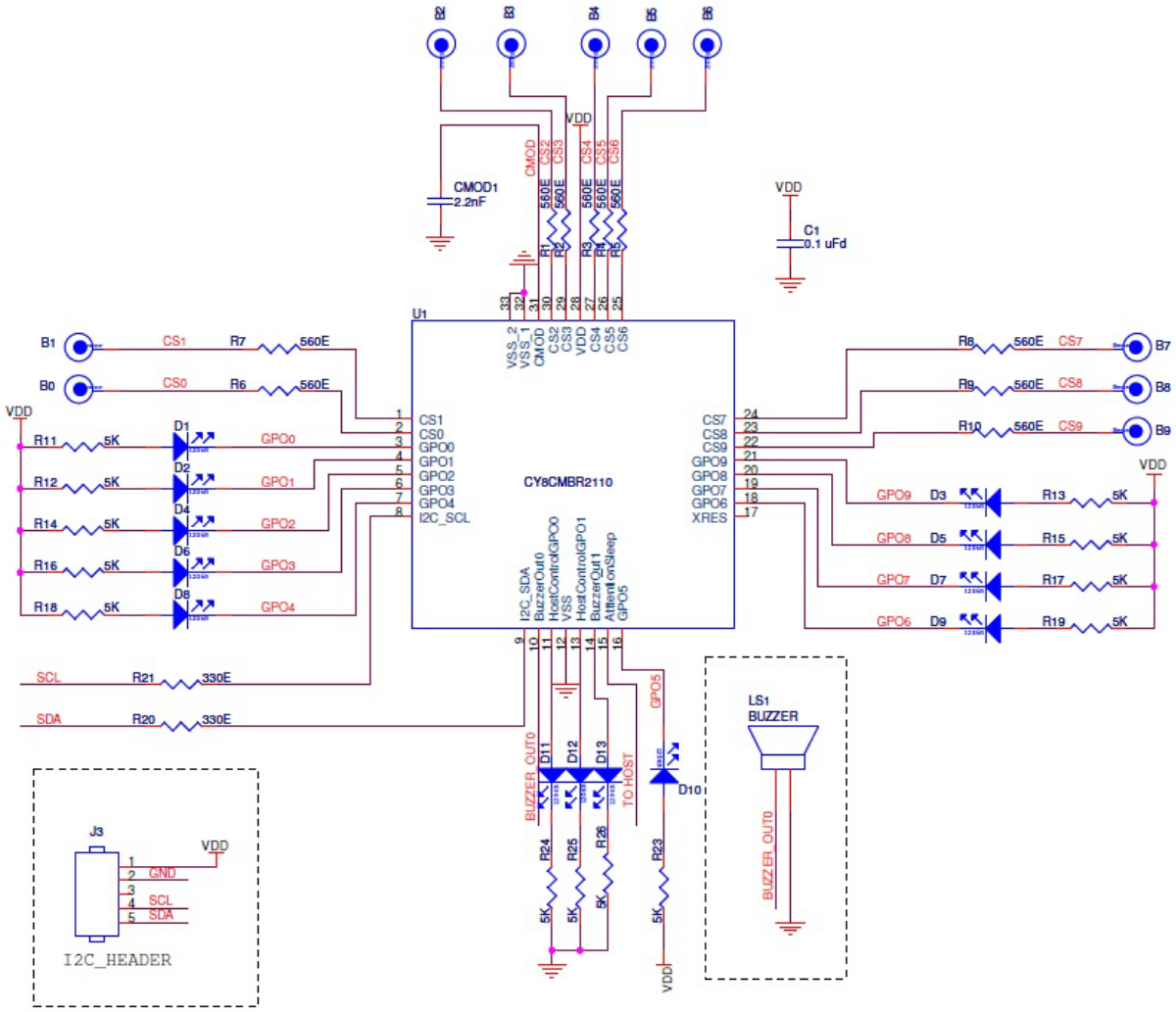


Note
2. AI – Analog Input; DI – Digital Input; DO – Digital Output; DIO – Digital Input / Output; P – Power

Typical Circuits

Schematic 1: Ten Buttons with Ten GPOs

Figure 1. CY8CMBR2110 Schematic 1

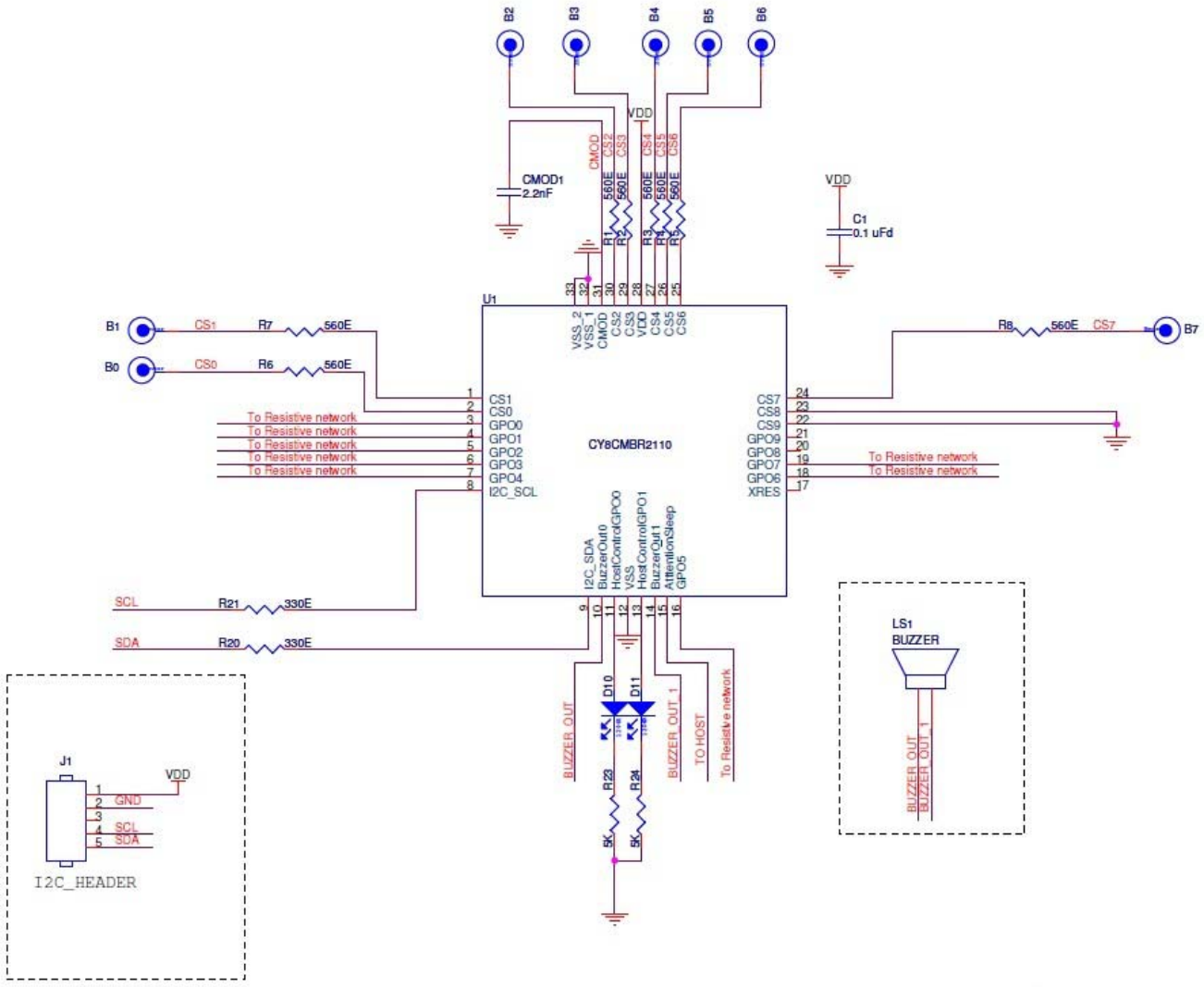


In Figure 1, the device is configured in the following manner:

- CS0–CS9 pins: 560 Ω to CapSense buttons
  - Ten CapSense buttons (CS0–CS9)
- GPO0–GPO9 pins: LED and 5 kΩ to V_{DD}
  - CapSense buttons driving 10 LEDs (GPO0-GPO9)
- C_{MOD} pin: 2.2 nF to ground
  - Modulating capacitor
- XRES pin: Floating
  - For external reset
- BuzzerOut0 pin: To buzzer
  - AC buzzer (1-pin)
  - Buzzer second pin to Ground
- BuzzerOut1 pin: LED and 5 kΩ to Ground
  - Used as Host Controlled GPO
- HostControlGPO0, HostControlGPO1: LED and 5 kΩ to Ground
  - Two Host Controlled GPOs
- HostControlGPO0, HostControlGPO1: Floating
  - Host Controlled GPOs disabled
- I2C_SDA, I2C_SCL pins: 330 Ω to I^2C header
  - For I^2C communication
- Attention/Sleep pin: To host
  - For controlling I^2C communication, power consumption, and device operating mode

Schematic 2: Eight Buttons with Analog Voltage Output

Figure 2. CY8CMBR2110 Schematic 2



In Figure 2, the device is configured in the following manner:

- CS0–CS7 pins: 560 Ω to CapSense buttons; CS8, CS9 pins: Ground
  - Eight CapSense buttons (CS0–CS9)
  - CS8 and CS9 buttons not used in design
- GPO0–GPO7: To external resistive network
  - Eight GPOs (GPO0–GPO7) used for Analog Voltage Output
  - GPO8 and GPO9 not used in design
- C_{MOD} pin: 2.2 nF to ground
  - Modulating capacitor
- XRES pin: Floating
  - For external reset
- BuzzerOut0 and BuzzerOut1 pins: To AC buzzer
  - AC Buzzer (2-pin)
- HostControlGPO0, HostControlGPO1 pins: LED and 5 kΩ to ground
  - Two Host-controlled GPOs
- I2C_SDA, I2C_SCL pins: 330-Ω to I^2C header
  - For I^2C communication
- Attention/Sleep pin: To Host
  - For controlling I^2C communication, power consumption, and device operating mode

Configuring the CY8CMBR2110

EZ-Click Customizer Tool

The EZ-Click Customizer tool is a simple and intuitive graphical user interface for efficiently configuring the device. It takes all the required parameters and configures the device accordingly, using I^2C communication. The configuration can be saved locally on the computer and later re-used by the tool for another design. The tool can also be used to generate a configuration file, which can be used through Bridge Control Panel (refer to AN2397 - CapSense Data Viewing Tools) or by the host (in the host firmware) to configure the device. For more details, refer to the EZ-Click Customizer Tool User Guide.

Configuring the Device using a Host Processor

CY8CMBR2110 can be configured by a Host processor. The advantages of using a host processor to configure are listed below.

- In-system configuration - no need to take the device (chip) out of the board.
- Run time configuration - modifying the features dynamically by a host processor.

To configure the device using a Host processor, there is a comprehensive list of APIs and these APIs are to be called from the Host processor in a specific order. These APIs use I2C communication to configure the device features. You can download the source code from http://www.cypress.com/?rID=74590.

For more details refer to CY8CMBR2110 CapSense® Design Guide.

Third-party Programmer

To configure large number of devices, Cypress recommends a third-party vendor to perform automated programming on the devices. For this, you must give the hex file of your configuration, generated by EZ-Click Customizer Tool to Hilo systems (a third-party programmer).

Contact http://www.hilosystems.com.tw/en/index.aspx for further information.

Device Features

CapSense Buttons

- Supports up to 10 CapSense buttons
- Ground the CSx pin to disable CapSense button input
- Connect a 2.2-nF (±10%) capacitor on the C_{MOD} pin for proper CapSense operation
- For proper CapSense operation, ensure C_P of each button is less than 40 pF

SmartSense Auto-Tuning

- Supports auto-tuning of CapSense parameters
- Does not require manual tuning; all parameters are automatically tuned by the device
- Reduces the design cycle time
  - No manual tuning
- Ensures portability of the user interface design
- Compensates printed circuit board (PCB) variations, device process variations, and PCB vendor changes

General Purpose Outputs (GPOs)

- GPOx pin outputs are strong drive[3]
- The GPOx is controlled by the corresponding CSx
- Active low output – supports sinking configuration for LEDs (see Figure 3)
- If CSx is disabled (grounded), then the corresponding GPOx must be left floating
- After power-up on the GPOx, a 5-ms pulse is sent after 350 ms (if Noise Immunity level is “Normal”) and 1000 ms (if Noise Immunity level is “High”), if the CSx fails the System Diagnostics

Figure 3. Example of GPO0 Driven by CS0

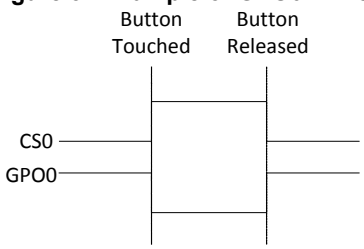


Table 2. CY8CMBR2110 Advanced Features

Feature	Benefits
Toggle ON/OFF	Button retains state after touch (ON/OFF)
Flanking Sensor Suppression (FSS)	Avoids multiple button trigger in a design with closely-spaced buttons
Noise Immunity	Improves device immunity to external noise (such as RF noise)
Automatic Threshold	Configurable finger threshold for different noise settings
LED ON Time	Gives an LED effect on button release
Button Auto Reset	Disables false output trigger when the conducting object is placed close to the button
Power-on LED Effects and Button Touch LED Effects	Provides visual effects to design at power-on and button touch
Standby Mode LED Brightness	Used for LED backlighting
Latch Status Read	No button touch missed by host processor
Attention/Sleep Line to Host	Provides device interrupt to host. Host can use this to read data from the device. Also controls device operating mode.
Analog Voltage Support	External resistors can be used with GPOs to generate analog voltage output
Sensitivity Control	Maintains optimal button performance for different overlay and noise conditions
Debounce Control	Prevents false trigger of buttons
Buzzer Signal Output	Provides audio feedback on button touch
Host Controlled GPOs	GPO pins, which can be controlled by the host processor through I^2C
System Diagnostics	Supports production testing and debugging
Low-Power Sleep Mode and Deep Sleep Mode	Low power consumption

Note
3. When a pin is in strong drive mode, it is pulled up to V_{DD} when the output is HIGH and pulled down to Ground when the output is LOW.

Toggle ON/OFF

- Toggles the GPO state at each button touch (see Figure 4).
- Use for mechanical button replacement (for example, wall switch).
- Toggle feature can be enabled on each CapSense button individually.

Flanking Sensor Suppression (FSS)

- Allows only one button to be in the TOUCH state at a time. You can distinguish TOUCH states for closely spaced buttons.
- If a finger contacts multiple buttons, only the first one to sense a TOUCH state turns ON.
- Also used in situations when a button can produce opposite effects. For example, an interface with two buttons for brightness control (UP or DOWN).
- FSS can be enabled for each button individually. This helps to enable FSS only for those buttons which are closely spaced. For example, if a design has ten buttons with six buttons closely-spaced, FSS can be enabled just for those six buttons.
- FSS action can be explained for the following scenarios:

1. When only one button is touched, it is reported as ON (see Figure 5).
2. When more than one button is detected as ON, and previously one of those buttons was touched, then the button touched previously is reported as ON (see Figure 6).

Noise Immunity

- Improves the immunity of the device against external radiated and conducted noise.
- Reduces the radiated noise emission.
- Possible Noise Immunity levels are “Normal” and “High”.
- Select “High” only in a high-noise environment because it increases device power consumption and response time.

Automatic Threshold

- Button Signal is compared to Finger Threshold for GPO output
- Finger Threshold is configurable; valid range is 50-245 counts
- Used to determine button ON/OFF state for different noise conditions
- You can configure Finger Threshold to be set automatically
- To learn more about Finger Threshold, refer to Section 2.3 in Getting Started with CapSense

Figure 4. Example of Toggle ON/OFF Feature on GPO0

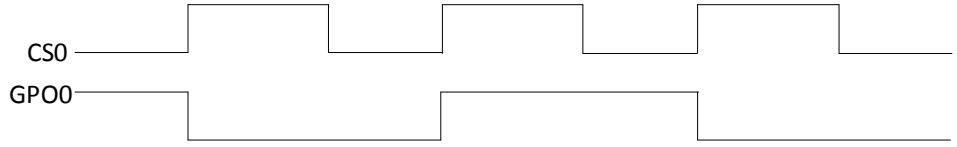
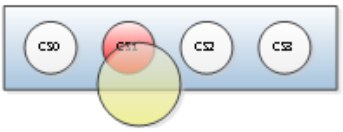


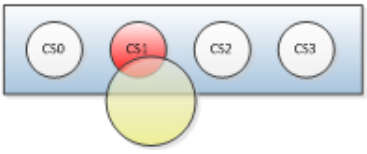
Figure 5. FSS when One Button is Touched

No button is ON Prior to the Touch

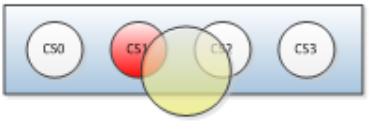


CS1 is Reported as ON Upon Touch

Figure 6. FSS when Multiple Buttons are Touched with One Button ON Previously



CS1 is touched; reported ON



CS2 also touched along with CS1;
CS1 is reported ON

LED ON Time

- Provides a variable amount of LED ON time (upto 5100 ms) after a button is released.
- The GPOx is driven low for a specified interval after the corresponding CSx button is released (see Figure 7).
- When a button is reset (refer to Button Auto Reset on page 10), LED ON Time is not applied on the corresponding GPO.
- Applicable to the GPO of the last button released
- In Figure 8, GPO0 goes high prematurely (prior to LED ON Time expiration) because CS1 button is released. Therefore, the LED ON Time counter is reset. Now, the GPO1 remains low for LED ON Time after releasing CS1.
- LED ON Time can range from 0-5100 ms.
- LED ON Time resolution is 20 ms.
- LED ON Time is disabled if Toggle ON/OFF is enabled.

Figure 7. Example LED ON Timing Diagram on GPO0

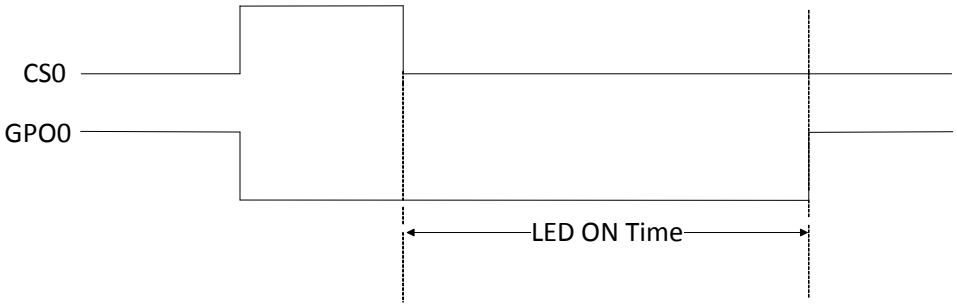
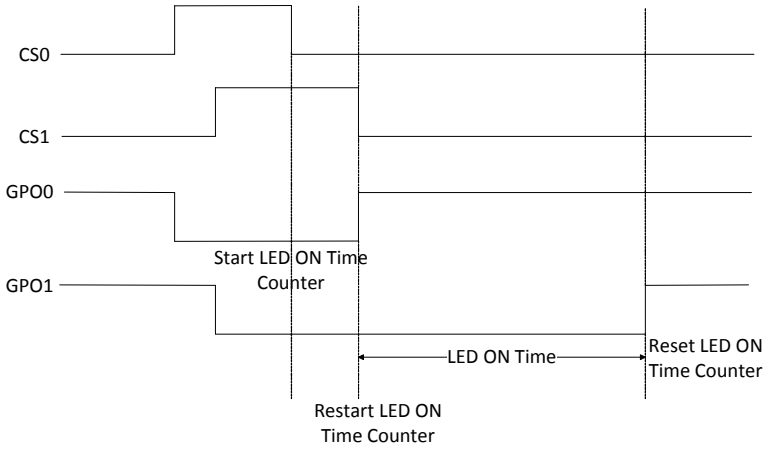


Figure 8. Example LED ON Timing Diagram on GPO0 and GPO1



Button Auto Reset

- Prevents a stuck button due to a metal object placed close to that button.
- Useful when the button is kept ON only for a specific period of time.
- If enabled, button is considered OFF after the Button Auto Reset period, even though the button continues to be touched. See Figure 9.
- Auto Reset period can be set to 5 or 20 seconds.

Power-on LED Effects

- Provides a visual effect at device power-up.
- After power-on, all the LEDs show dimming and fading effects for an initial time.
- Seen on GPOx when CSx is enabled.
- The GPOs are configured in groups to have the same parameters.
- The groups are:
  - GPO1, GPO2, GPO3
  - GPO4, GPO5, GPO6
  - GPO7, GPO8, GPO9
- GPO0 can be configured separately. Useful in designs with a special use for CS0 button, such as a power button.
- All CapSense buttons are disabled during this time.
- If any CapSense button (CSx) fails the Power-on Self Test, then these effects are not seen on the corresponding GPOx.
- To know more about Power-on Self Test, refer System Diagnostics on page 17.
- The following parameters are set for LED effects:
  - Low brightness – Minimum LED intensity
  - Low-brightness time – The time period for which the LED remains in a low-brightness state
  - Ramp-up time – The time period during which the LED transitions from low brightness to high brightness
  - High brightness – Maximum LED intensity
  - High-brightness time – The time during which the LED stays in a high-brightness state
  - Ramp-down time – The time it takes the LED to go from high brightness to low brightness
  - Repeat rate – The number of times the effects are repeated
- Brightness levels can range from 0 to 100 percent.
- The time range can be 0 to 1600 ms.
- High-brightness level must be more than low-brightness level.
- The effects are seen after the device initialization time from power-on. This time is less than 350 ms (if the Noise Immunity level is “Normal”) and less than 1000 ms (if the Noise Immunity level is “High”).
- The pattern can be set to occur sequentially or concurrently on all the GPOs (see Figure 10 and Figure 11 on page 11).
- During Power-on LED Effects, the device ACKs I^2C communication but all write commands are ignored. The Host can only read Operating mode data.

Figure 9. Example of Button Auto Reset on GPO0

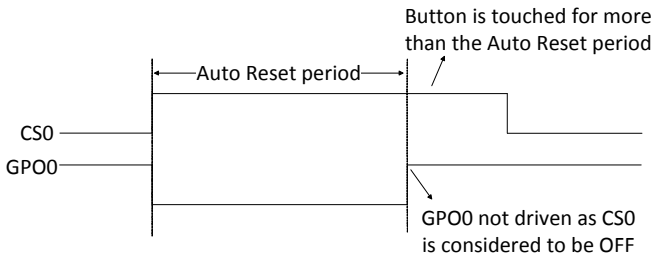


Figure 10. Example Power-on LED Effects (Concurrent on all GPOs) with Repeat Rate = 1[4]

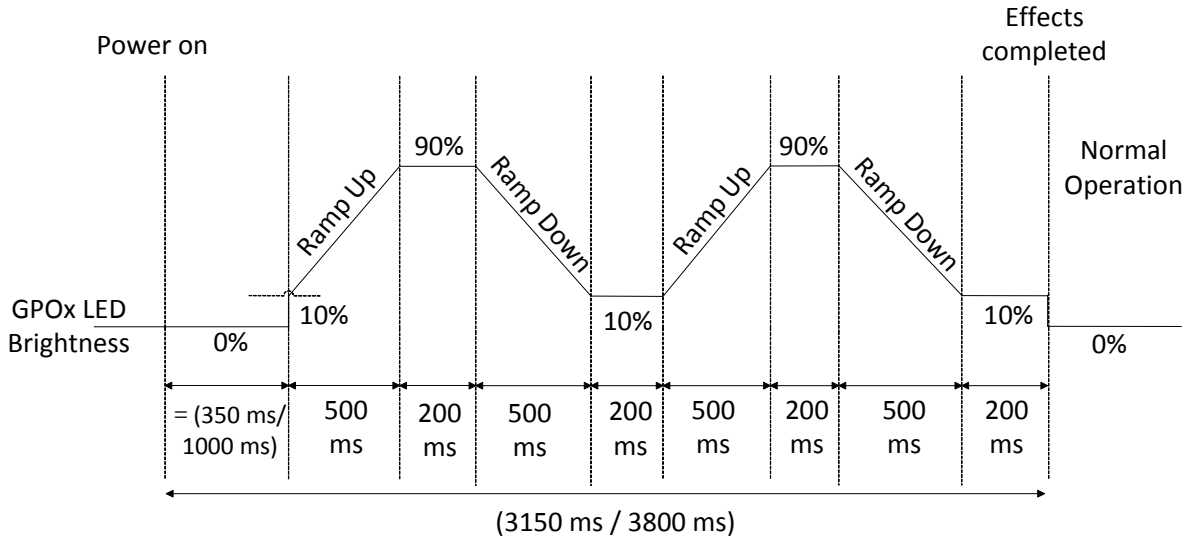
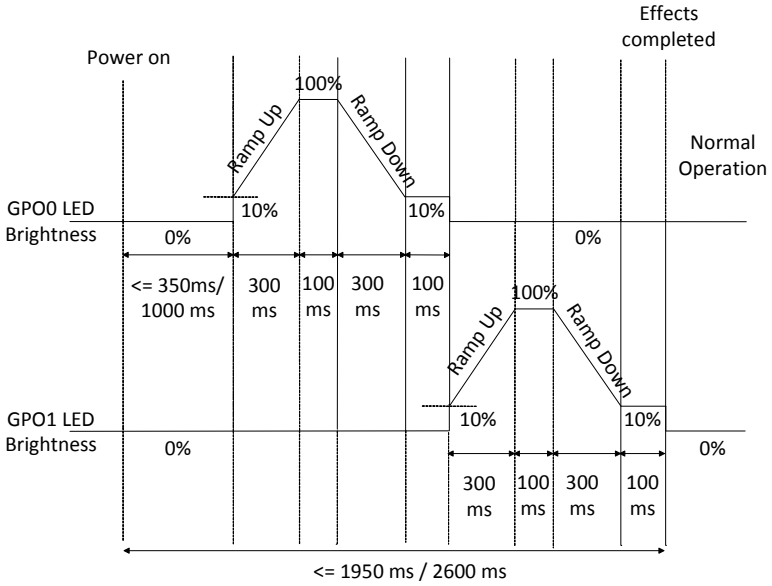


Figure 11. Example Power-on LED Effects (Sequential) with Two-Button Design and Repeat Rate = 0[5]



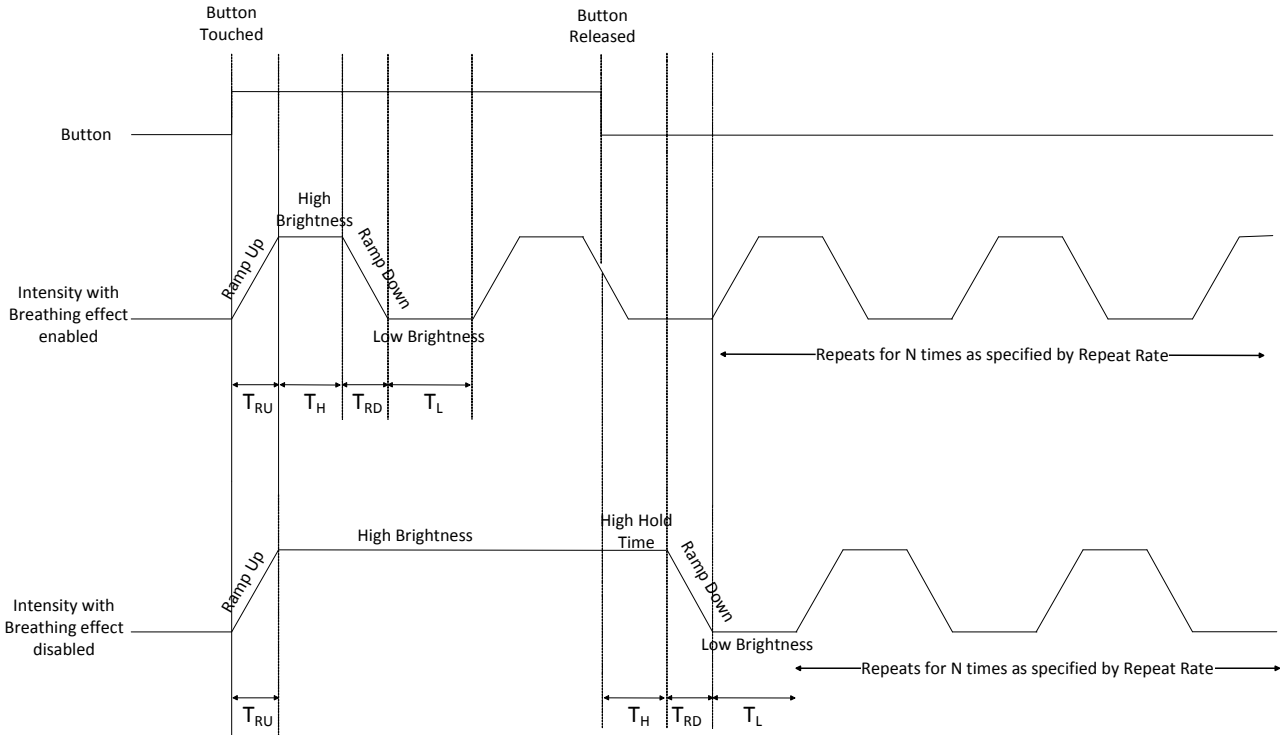
Notes

4. Ramp up time = 500 ms; High brightness = 90%; High brightness time = 200 ms; Ramp down time = 500 ms; Low brightness = 10%; Low brightness time = 200 ms; Repeat rate = 1
5. Ramp up time = 300 ms; High brightness = 100%; High brightness time = 100 ms; Ramp down time = 300 ms; Low brightness = 10%; Low brightness time = 100 ms; Repeat rate = 0

Button Touch LED Effects

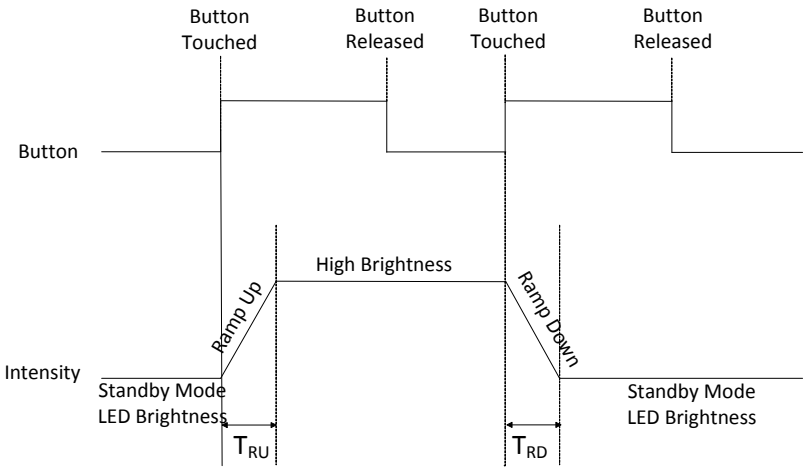
- Provides a visual feedback on a button touch. Improves the aesthetic value of the design.
- Seen on GPOx when CSx is touched.
- The GPOs are configured in groups to have the same parameters. The groups are:
  - GPO1, GPO2, GPO3
  - GPO4, GPO5, GPO6
  - GPO7, GPO8, GPO9
- GPO0 can be configured separately. Useful in designs with a special use for the CS0 button, such as the power button.
- The following parameters can be set for the effects:
  - Low brightness – Minimum LED intensity
  - Low-brightness time – The time period during which LED remains in a low-brightness state
  - Ramp-up time – The time period during which the LED transitions from low brightness to high brightness
  - High brightness – Maximum LED intensity
  - High-brightness time – The time during which the LED stays in a high-brightness state
  - Ramp-down time – The time it takes the LED to go from high brightness to low brightness
  - Repeat rate – The number of times the effects are repeated
- Brightness levels can range from 0 to 100 percent.
- The time range can be 0 to 1600 ms.
- High-brightness level should be more than the low-brightness level for proper visual effects.
- Button Touch LED effects can be of two types (see Figure 12 on page 12):
  - Breathing effects: When the breathing effect is enabled, LED intensity changes from Standby Mode LED Brightness to Low Brightness immediately after a button touch. It then ramps up to high-brightness and stays for high brightness time. It then ramps down to low brightness and stays for low brightness time. This effect repeats for the duration during which the button is touched. When the button is released, the LED effects cycle that is in progress, continues. After this cycle completes, the LED effects cycle may repeat depending on the Repeat Rate.
  - Non-breathing effects: When the breathing effect is disabled, the LED intensity changes from Standby Mode LED Brightness to Low Brightness immediately after a button touch. It then ramps up to high brightness and stays there for the duration during which the button is touched. When the button is released, the LED maintains its state for high brightness time. It then ramps down to low brightness and stays for low brightness time. This effect may then repeat depending on the repeat rate.
- If the Button Touch LED Effects are active on one GPOx and the corresponding CSx is touched again, then the pattern restarts on GPOx.
- If the Toggle ON/OFF effect is also enabled, the LEDs toggle between Standby Mode LED Brightness and High Brightness on successive button touches (see Figure 13 on page 13).
- If Button Touch LED Effects are enabled, the LED ON time is automatically disabled.
- When the device goes to Deep Sleep, ongoing Button Touch LED Effects are immediately disabled.

Figure 12. Button Touch LED Effect Pattern[6]



Note
6. T_{RU} – Ramp Up Time; T_{RD} – Ramp Down Time; T_H – High Brightness Time ; T_L – Low Brightness Time

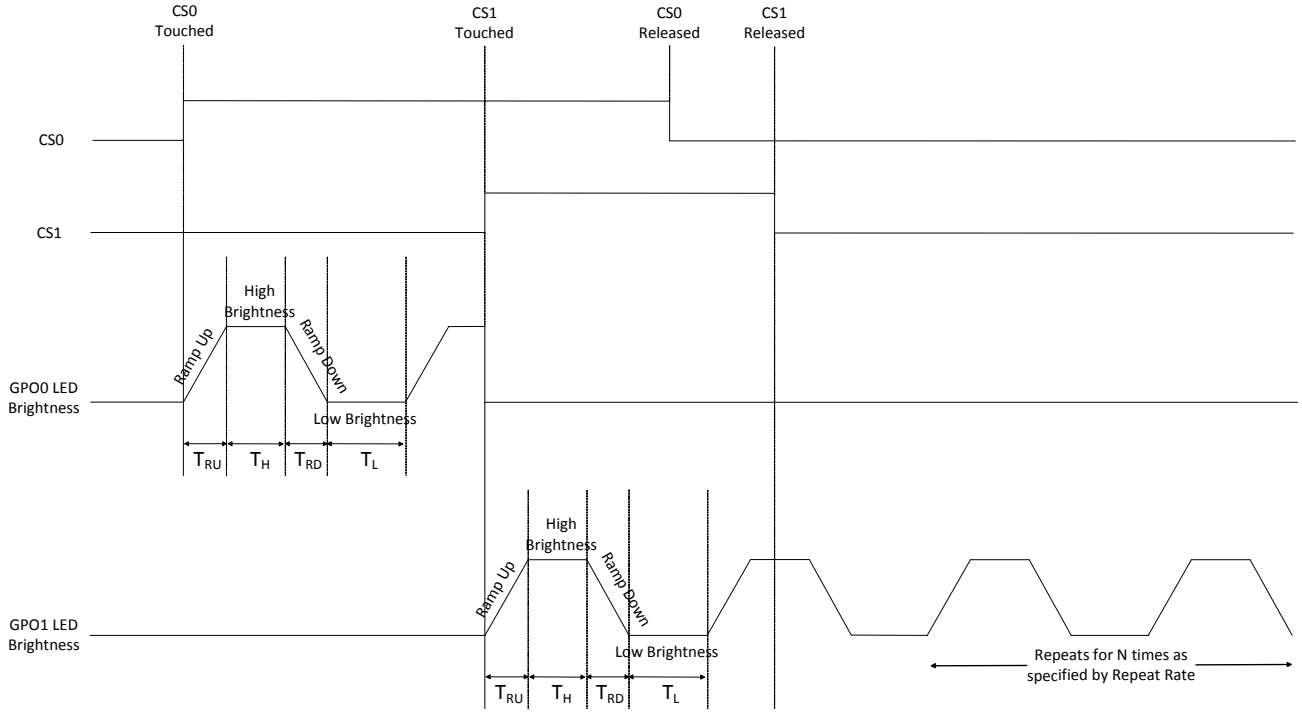
Figure 13. Button Touch LED Effects with Toggle Enabled



Last Button LED Effect

- Button Touch LED Effects can be configured to be interrupted on one GPO if any other button is touched.
- The effects reset on the first GPO and start on the GPO associated with the last button touched (see Figure 14).
- This feature is disabled by default.
- If Toggle ON/OFF is also enabled for some buttons, Last Button LED Effect is disabled for those buttons.
- If the Flanking Sensor Suppression (FSS) feature is also enabled, and two buttons are touched simultaneously, the Last Button LED Effect does not apply because the second button touched does not turn ON.

Figure 14. Button Touch LED Effects (Breathing) with Last Button LED Effect Enabled



Standby Mode LED Brightness

- Provides a better visual feedback for buttons when in OFF state. Improves the aesthetic value.
- The LED associated with GPOx is in Standby Mode LED Brightness after the conclusion of Button Touch LED Effects, when CSx is OFF.
- Standby Mode LED Brightness can be configured to be 0%, 20%, 30%, or 50%.
- Standby Mode LED Brightness increases device power consumption because the device does not go to Low Power Sleep.
- Standby Mode LED Brightness is disabled when the device goes to Deep Sleep.

Latch Status Read

- Host processor can check the CapSense button status by reading the Register Map through I^2C communication.
- When a button is touched, the device generates an interrupt to host through the Attention/Sleep line. Host can then read CSx status.
- If the interrupt is not serviced immediately, and the button is released before the interrupt is serviced, the host can miss that button touch.
- To avoid missing any button touch, the host should read both current status (CS) and latch status (LS).
- CS is stored in the Button_Current_Stat0 and Button_Current_Stat1 registers in Operating Mode.
- LS is stored in the Button_Latch_Stat0 and Button_Latch_Stat1 registers in Operating Mode.
- To know more about these registers, refer to Operating Mode.
- Table 3 on page 14 lists the various possibilities of button touch acknowledge/miss. These are shown in Figure 15 and Figure 16.

Table 3. Latch Status Read

Current Status (CS)	Latch Status (LS)	Comments
0	0	CSx is not touched during the current I^2C read; Host has already acknowledged any previous CSx touch in the last I^2C read.
0	1	CSx was touched before the current I^2C read; this CSx touch was missed by the host.
1	0	CSx was touched and acknowledged by the host during the previous I^2C read; the same CSx is still touched during the current I^2C read.
1	1	CSx is touched during the current I^2C read.

Figure 15. Latch Status Read 1

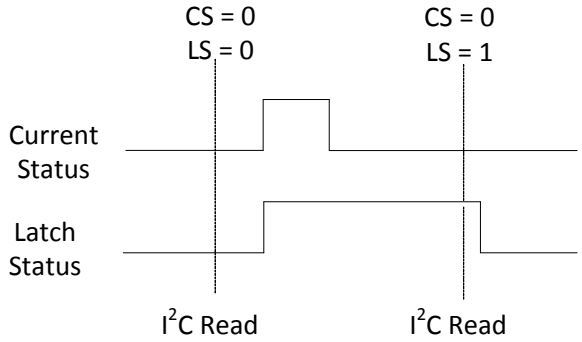
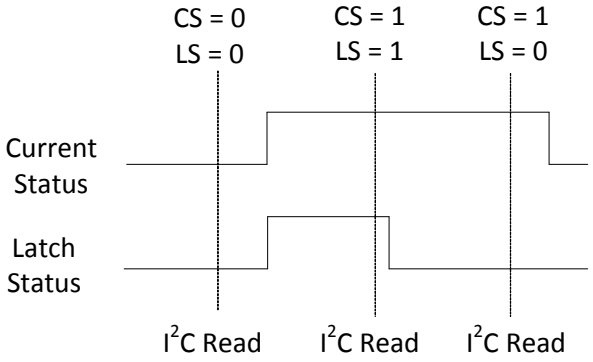


Figure 16. Latch Status Read 2



Attention/Sleep Line to Host

- Bidirectional active low line; can be controlled by both the device and the host.
- The Attention/Sleep line is in the Open Drain Low Drive mode
- The device is in the low-power Sleep mode by default (if the attention/sleep line is high). For more information, refer to the section Low-Power Sleep Mode on page 21.
- The device cannot go to the low-power Sleep mode if the attention/sleep line is low.
- Attention/Sleep line should be pulled low only if required, to reduce device power consumption.

Attention/Sleep line can be used for the following functions:

Device Interrupt to Host

- On any button touch, the device pulls the Attention/Sleep line low to indicate an interrupt to the host (see Figure 17 on page 15).
- If more than one button is touched simultaneously, the attention line is pulled low for the entire duration of any button touch (see Figure 18 on page 15).
- The Attention/Sleep line goes high when the button is released.

Figure 17. Attention/Sleep Line with CSx Buttons Touched Separately

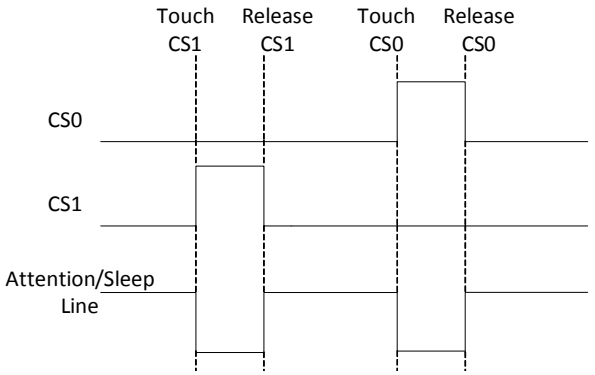
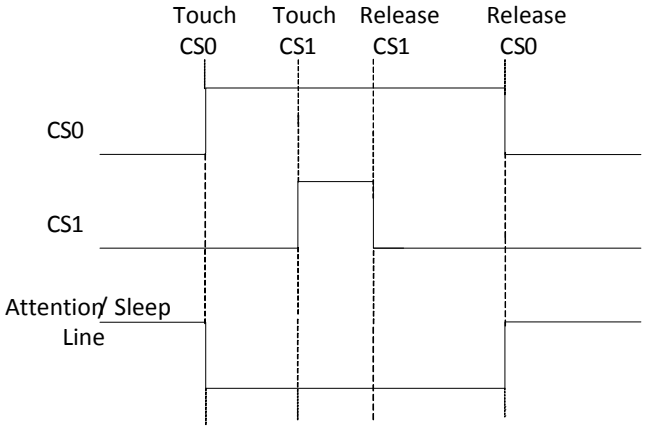


Figure 18. Attention/Sleep Line with CSx Buttons Touched Simultaneously



I^2C Communication

- Attention/Sleep line should be pulled low before any I^2C communication is initiated.
- If the Attention/Sleep line is high, the device may NACK I^2C communication.
- When the Attention/Sleep line is low, the device may NACK I^2C communication, but very infrequently.

Deep Sleep mode

- To enable the Deep Sleep mode, the host needs to set the “Deep Sleep” bit in Host_Mode register (in the Operating Mode). The host needs to wait for 50 ms and then pull Attention/Sleep line high.
- Host should pull the Attention/Sleep line low for the device to wake up from deep sleep.
- For more information, refer to the section Deep Sleep Mode on page 21.

Analog Voltage Support

- A general external resistive network with a host processor is shown in Figure 19.
- Host can be configured to perform different functions based on the voltage level at input pins. This is controlled by switches.
- These switches can be controlled by CapSense buttons.
- If enabled, GPOs replace these switches in the network.
- GPOs are in the Open Drain Low Drive mode.
- GPOs cannot be used for the resistive network and LED drive simultaneously.
- If only one button needs to be ON for analog voltage support, FSS should be enabled.
- For CY8CMBR2110, a simple external resistive network is shown in Figure 20.

Figure 19. General External Resistive Network

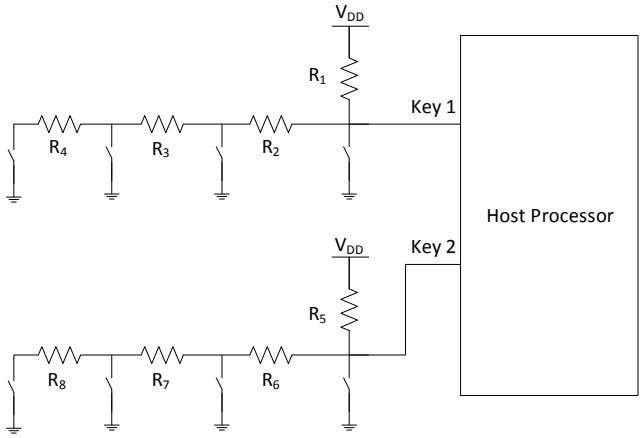
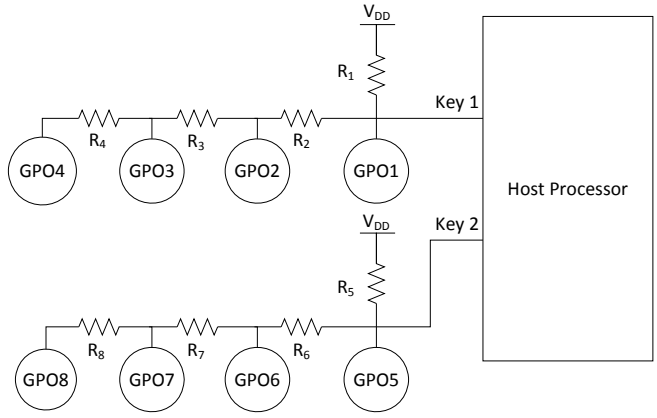


Figure 20. Analog Voltage Support for CY8CMBR2110



Sensitivity Control

- Sensitivity of each button can be set individually.
- Use higher sensitivity setting when the overlay thickness is higher or if the button diameter is small.
- Use a lower sensitivity setting when power consumption needs to be low.
- Possible sensitivity settings are “High”, “Medium”, and “Low”.

Debounce Control

- Avoids false triggering of buttons due to noise spike or any other glitches in the system.
- Specifies the minimum time for which a button has to be sensed as touch, for an output trigger. Debounce value can range from 1 to 255.
- Debounce value can be set separately for CS0 and combined for CS1 to CS9. This is useful for additional functions, such as, linking system reset to touch time corresponding to CS0 Debounce.
- The device Response Time depends on the button debounce. Refer to Response Time on page 22.

Table 4 lists some examples of device Response Time for different debounce values.[7]

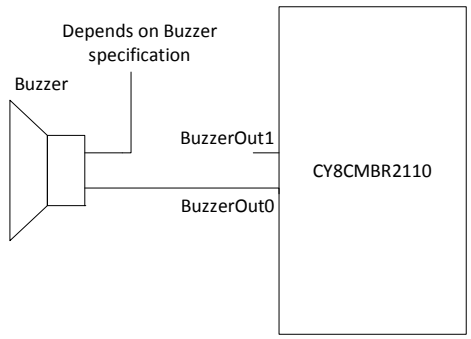
Table 4. Example Response Times for Debounce Values

Debounce Value	Response Time for Consecutive Button Touch (ms)
1	70
4	105
7	140
10	175
100	1225
200	2380
255	3010

Buzzer Signal Output

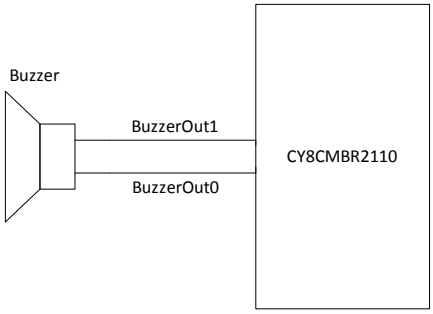
- Gives audio feedback for a button touch. For more details, refer to Response Time on page 22.
- Buzzer signal output can have two configurations: AC 1-pin and AC 2-pin.
- In the AC 1-pin buzzer configuration, the buzzer must be connected to the BuzzerOut0 pin (see Figure 21). A square wave of the given frequency and duty cycle is driven on this pin. The BuzzerOut1 pin can either be left floating or configured as a Host-controlled GPO.

Figure 21. AC 1-Pin Buzzer Configuration



- In AC 2-pin buzzer configuration, connect the buzzer between the BuzzerOut0 and BuzzerOut1 pins (see Figure 22). Two out-of-phase square waves of the given frequency and duty cycle are driven on these pins.

Figure 22. AC 2-Pin Buzzer Configuration



- If the buzzer is not used, then both the pins can be used as Host-controlled GPOs. Table 5 shows the possible buzzer settings.
- The idle state of the buzzer pin can be configured to be either V_{DD} or Ground.
- The buzzer pin is driven to the idle state when no button is touched, or after the Buzzer ON Time elapses, even when the button is kept touched (see Figure 23).
- The buzzer signal frequency is configurable and can assume one of the following values (in kHz) – 1.00, 1.14, 1.33, 1.60, 2.00, 2.67, 4.00
- The buzzer output is driven for the configured time and does not depend on the button touch time.
- Buzzer ON Time has a range of (1 to 127) × Button Scan Rate constant. To know more about Button Scan Rate constant, refer to Power Consumption and Operating Modes on page 21.
- Buzzer Signal Output is strong drive.
- The output is driven commonly by all the CSx buttons.
- Buzzer output restarts if any button is touched before the Buzzer ON time expiration (see Figure 24).

Note
7. 8-buttons, Noise Immunity level Normal, Response Time optimized design.

Figure 23. Buzzer Time-out

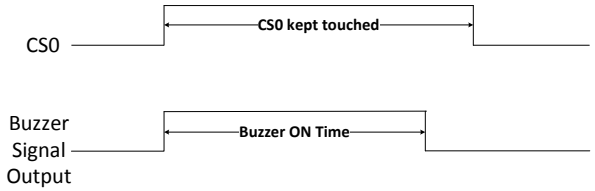


Figure 24. Buzzer Terminated and Restarted

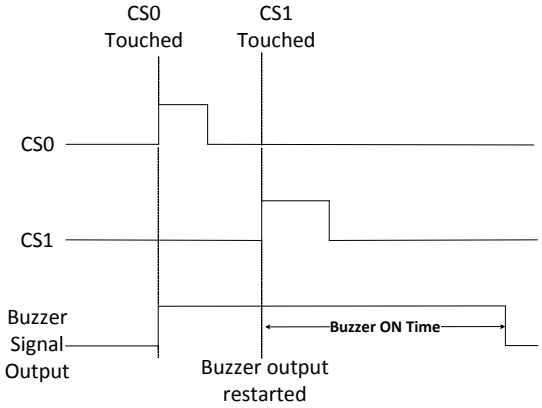


Table 5. Buzzer and Host-Controlled GPO Settings

Buzzer Configuration	BuzzerOut0 Pin	BuzzerOut1 Pin	Max Available Host Controlled POs
No Buzzer	Floating/Host Controlled GPO3	Floating/Host Controlled GPO2	4
AC 1-pin buzzer	Buzzer pin 0	Floating/Host Controlled GPO2	3
AC 2-pin buzzer	Buzzer pin 0	Buzzer pin 1	2

Host Controlled GPOs

- Two GPO pins (HostControlGPO0, HostControlGPO1) are available whose logic states can be controlled by the host.
- If the buzzer is not used, then up to two more host-controlled GPOs are available (using BuzzerOut0 and BuzzerOut1 pins).
- The Host can control these GPOs in the Operating mode, Production Line Test mode, and Debug Data mode.
- Host-controlled GPOs are in LOW state at power-on.
- Host-controlled GPO settings cannot be saved to flash and must be configured after reset.
- HostControlGPO1 has a positive going pulse of 16 ms during power-on.
- These outputs are in strong drive mode.
- Table 5 shows the maximum available Host-Controlled GPOs, depending on the buzzer configuration.

System Diagnostics

- A built-in Power-on Self Test (POST) mechanism performs some tests at power-on reset (POR), which can be useful in production testing.
- If any button fails these tests, a 5-ms pulse is sent out on the corresponding GPO within 350 ms (if Noise Immunity level is “Normal”) or 1000 ms (if Noise Immunity level is “High”) after POR.
- To know the System Diagnostics result, the host can read device data in Production Line Test mode through the I^2C interface.
- Since the host can read data through I^2C lines, there is no need to interface GPOs to the host.

The following tests are performed on all the buttons.

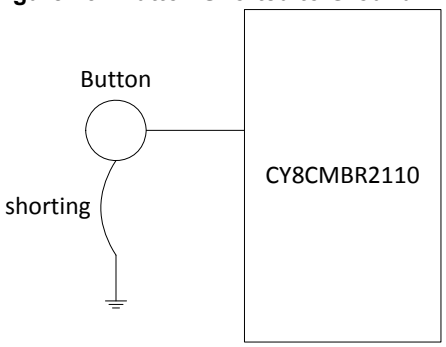
Button Shorted to Ground

If any button is shorted to ground, it is disabled. For an accurate detection of Button Shorted to Ground, the resistance between the CSx pin and ground should be less than the limits specified in Table 6.

Table 6. Maximum Resistance between CSx and GND for Proper System Diagnostics Operation

Power supply (V_{DD}) (V)	Max resistance between CSx and GND (Ω)
5.5	680
5	760
1.8	1700

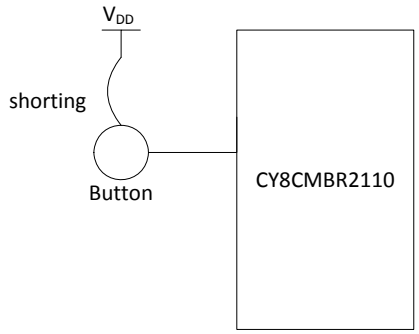
Figure 25. Button Shorted to Ground



Button Shorted to V_{DD}

If any button is shorted to V_{DD}, it is disabled.

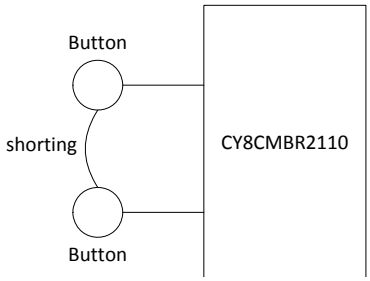
Figure 26. Button Shorted to V_{DD}



Button to Button Short

If two or more buttons are shorted to each other, all of these buttons are disabled.

Figure 27. Button to Button Short



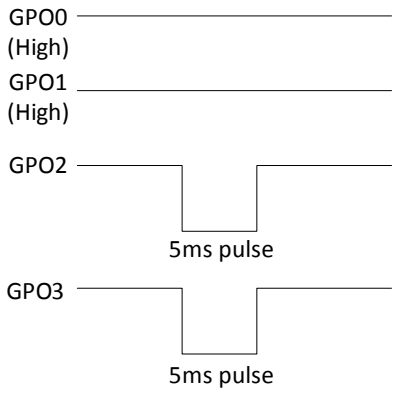
Improper Value of C_{MOD}

- Recommended value of C_{MOD} is 2 nF to 2.4 nF.
- If the value of C_{MOD} is less than 1 nF or greater than 4 nF, all the buttons are disabled.

Button C_P > 40 pF

If the parasitic capacitance (C_P) of any button is more than 40 pF, that button is disabled.

Figure 28. Example Showing CS0 and CS1 Passing the POST and CS2 and CS3 Failing



In Figure 28, CS0 and CS1 are enabled; CS2 and CS3 are disabled because they failed the POST. Therefore, a 5-ms pulse is observed on GPO2 and GPO3.

I²C Communication

I²C is the interface used to communicate between the CY8CMBR2110 (I²C slave) and the host (I²C master). It uses a simple two-wire synchronous communication protocol. These two wires are:

1. Serial Clock (SCL) – This line is used to synchronize the slave with the master.
2. Serial Data (SDA) – This line is used to send data between the master and the slave.

The CY8CMBR2110 can be a part of a one-slave or a multi-slave environment. See Figure 29 and Figure 30.

Figure 29. I²C Communication between One Master and One Slave

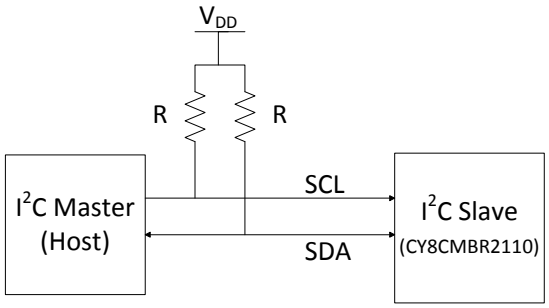
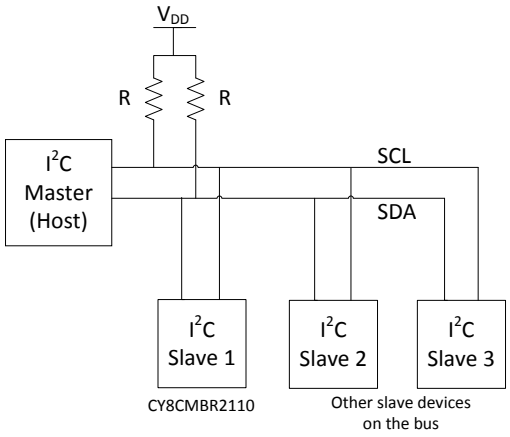


Figure 30. I²C Communication between One Master and Multiple Slaves



The CY8CMBR2110 I²C interface has the following features:

1. Bit rate up to 100 kbps
2. Configurable I²C slave address (0–127), with default slave address as '37h'.
3. Hardware address compare
4. No bus-stalling – No clock stretching
5. I²C buffer mode (32-byte hardware buffer)
6. Register-based access to I²C master for read and write operations.

I²C Slave address

To uniquely identify each device in a multi-device state, an I²C slave address is used. This address is a 7-bit value, which allows up to 127 slaves on the bus simultaneously. When the bus master wants to communicate with a slave on the bus, it sends a start condition followed by the I²C address of the relevant slave. The start condition alerts all slaves on the bus when a new transaction starts. The slave with the specified I²C address acknowledges the master. All the other slaves ignore all further traffic on the bus until the next start condition is detected.

Start and Stop Conditions

The master initiates the communication by issuing a START condition on the bus and terminates the communication by issuing a STOP condition. The bus is considered busy between these two conditions. See Figure 31.

A START condition is shown by changing the level of SDA line (from high to low), when the SCL line is high.

A STOP condition is shown by changing the level of SDA line (from low to high), when the SCL line is high.

Figure 31. I²C START and STOP Conditions

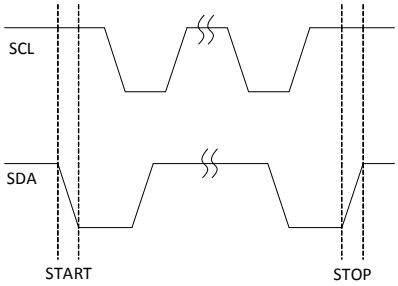
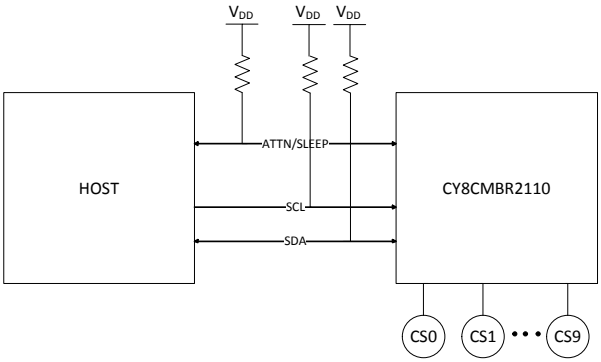


Figure 32. I²C Interface between Host and Device



I²C Communication Guidelines for CY8CMBR2110

1. The Attention/Sleep line should be pulled low by either the host or the device, before initiating any I²C communication.
2. The host needs to wait for 350 ms (if Noise Immunity level is “Normal”) or 1000 ms (if Noise Immunity level is “High”) after device power-on, before initiating any I²C communication. Else, the device NACKs any such communication.
3. The host needs to wait for a minimum of 60 ms after any I²C transaction before initiating a new transaction.
4. Host needs to wait for 350 ms (if Noise Immunity level is “Normal”) or 1000 ms (if Noise Immunity level is “High”) after “Save to flash” and “Software reset” commands are issued before initiating any further transaction.
5. In run time the device should be in Operating mode.
6. The host should not initiate a new START condition for the device, without a STOP condition for the previous I²C communication (also called REPEAT START condition).
7. Host needs to maintain a minimum of 60 ms between any two I²C transactions
   a. If the host does not maintain this time while reading, then it gets the same data as read in previous transaction.
   b. If the host writes to the same register twice within this time, then the old data is lost.
   c. If the host writes to different registers within this time (reg x in first write and reg y in second write) then the data is not lost.

Write Operation

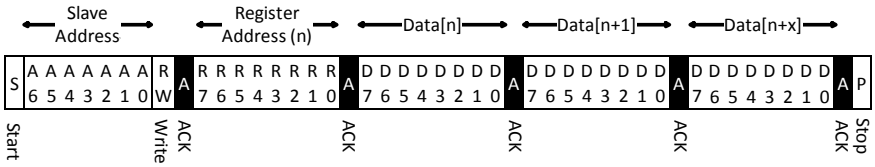
For a write operation, the following steps are performed:

1. The Host sends the START condition to the device on the SDA line.
2. The Host specifies the slave address, followed by R/W bit to specify a write operation. The device ACKs the Host.
3. The Host specifies the register address to which it has to write. The device ACKs the Host.
4. The Host starts sending the data to the device, which is written to the register address specified by the host. This is followed by an ACK from the device.
5. If the write operation includes more bytes, each following byte is written to the successive register address. Each successive byte is followed by an ACK from the device.
6. After the write operation is complete, the Host sends the STOP condition to the device. This marks the end of the communication. See Figure 33 on page 20.

Notes

1. The Host must not write to a Read Only register.
2. The Host can write a maximum of 32 bytes in one I²C transaction.

Figure 33. Host Writing x Bytes to the Device

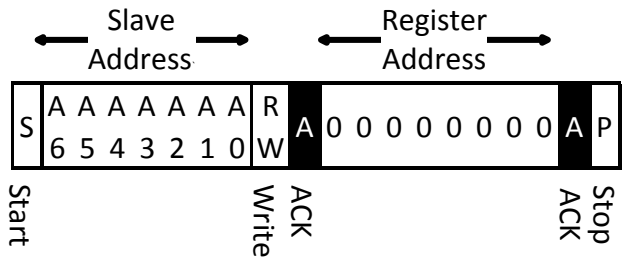


Setting the Device Data Pointer

The Host sets the device data pointer to specify the starting point for future read operations. To set the device pointer, perform the following steps:

1. The Host sends the START condition to the device on the SDA line.
2. The Host specifies the slave address on the SDA line, followed by the Read/Write bit to specify a write operation. The device ACKs the Host.
3. The Host specifies a register address (this register address is always 00). Any future read operations start from this address in the device. The device ACKs the Host.
4. The Host sends the STOP condition to the device. This marks the end of the communication. See Figure 34.

Figure 34. Host Setting the Device Data Pointer

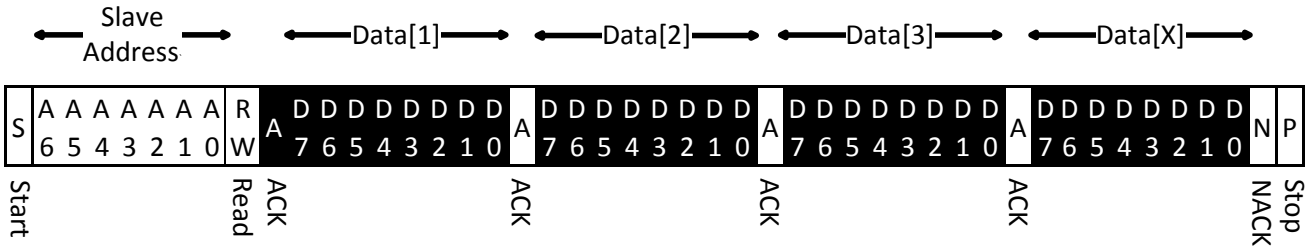


Read Operation

For a read operation, perform the following steps:

1. The Host sends the START condition to the device on the SDA line.
2. The Host specifies the slave address, followed by the Read/Write bit to specify a read operation. The device ACKs the Host.
3. The device retrieves the byte from the register address 00 and sends it to the Host. The Host ACKs the device.
4. Each successive byte is retrieved from the successive register address and sent to the Host, followed by ACKs from the Host.
5. After the host has received the required bytes, it NACKs the device.
6. The Host sends the STOP condition to the device. This marks the end of the communication. See Figure 35.

Figure 35. Host Reading x Bytes from the Device



Legend

CY8CMBR2110 to Host
HOST to CY8CMBR2110

For I^2C electrical specifications of the device, refer to the I2C Specifications.

Power Consumption and Operating Modes

CY8CMBR2110 can meet low-power requirements of battery-powered applications. To design for the lowest operating current, do the following:

- Ground all unused CapSense inputs (CSx).
- Minimize C_P using the design guidelines in Getting Started with CapSense, section 3.7.1.
- Reduce supply voltage (valid range: 1.71 V to 5.5 V).
- Reduce the sensitivity of CSx buttons.
- Configure the design to be optimized for power consumption.
- Use 'High' Noise Immunity level only if needed.
- Use a higher Button Scan Rate or Deep Sleep operating mode.

To know more about the steps to reduce power consumption, refer to section 5 in the CY8CMBR2110 Design Guide.

Low-Power Sleep Mode

The following flowchart describes the Low-Power Sleep mode operation.

- The Button Scan Rate is equal to the sum of the time the device scans and sleeps.
- The register settings define a Button Scan Rate offset.
- The offset is added to a constant to get the Button Scan Rate.
- The constant is given in Table 7.
- The range of scan rate is 25 to 561 ms.

Figure 36. Low Power Sleep Mode Operation

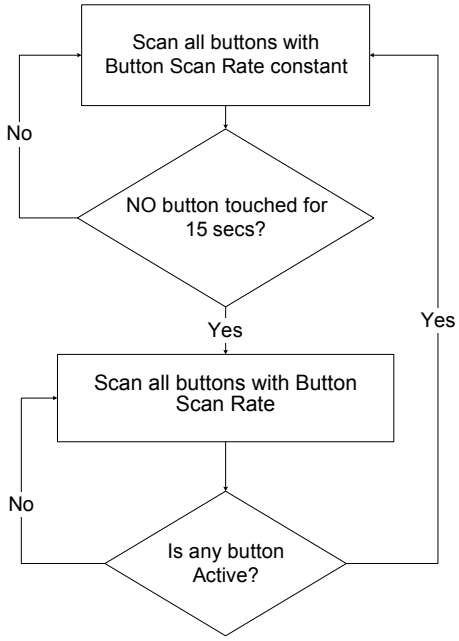


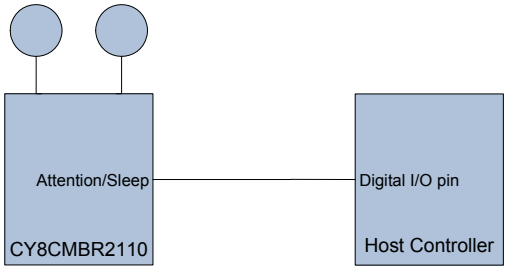
Table 7. Button Scan Rate Constant

Button Count	Button Scan Rate Constant			
	Response Time Optimized Design		Power Consumption Optimized Design	
	Noise Immunity Level "Normal"	Noise Immunity Level "High"	Noise Immunity Level "Normal"	Noise Immunity Level "High"
≤ 5	25 ms	35 ms	35 ms	55 ms
> 5	35 ms	55 ms	35 ms	55 ms

Deep Sleep Mode

- To enable the Deep Sleep mode, connect the Attention/Sleep line to the host as shown in Figure 37; the host should perform the following steps:
  - Pull the Attention/Sleep line low
  - Set the Deep Sleep bit in the Host_Mode register (in Operating Mode) high
  - Wait for 50 ms
  - Pull the Attention/Sleep line high

Figure 37. Attention/Sleep pin Connection to Enable Deep Sleep Mode



- In Deep Sleep mode, all blocks are turned off and the device power consumption is 0.1 µA.
- There is no CapSense scanning in Deep Sleep mode.
- After the device enters Deep Sleep mode, the 'Deep Sleep' bit is automatically cleared.
- The Attention/Sleep line should be pulled low for the device to wake up from Deep Sleep.
- When device comes out of Deep Sleep mode, the CapSense system is re-initialized. The typical time for re-initialization is 20 ms (Normal Noise Immunity level) or 50 ms (High Noise Immunity level). Any button touch within this time is not reported.
- The Deep Sleep bit cannot be set by EZ-Click Customizer Tool and must be set by an external I^2C communication to the device.

Response Time

Response time is the minimum amount of time the button should be touched for the device to detect as a valid button touch.

It is given by the following equations:

1. If Noise Immunity Level is “Normal”

.

$$RT_{CBT} = Button\ Scan\ Rate\ constant + \left[Button\ Scan\ Rate\ constant \times \left\{Round_{down}\left((Debounce - 1)/3\right) + 1\right\}\right]$$

$$RT_{FBT} = Button\ Scan\ Rate + \left[Button\ Scan\ Rate\ constant \times \left\{Round_{down}\left((Debounce - 1)/3\right) + 1\right\}\right]$$

2. If Noise Immunity level is “High”.

$$RT_{CBT} = Button\ Scan\ Rate\ constant + \left[Button\ Scan\ Rate\ constant \times Debounce\right]$$

$$RT_{FBT} = Button\ Scan\ Rate + \left[Button\ Scan\ Rate\ constant \times Debounce\right]$$

Where

RT_{CBT} is Response time for consecutive button touch after first button touch

RT_{FBT} is Response time for First button touch

Debounce for CS1-CS9 can be from 1 to 255

Debounce for CS0 can be from 1 to 255

$Round_{down}$ is the greatest integer less than or equal to ((Debounce – 1)/3)

Refer to Table 7 on page 21 to obtain Button Scan Rate constant.

For example, consider an eight-button, Response Time-optimized design with the Button Scan Rate offset set to 391 ms. The Noise Immunity level is set to Normal.

Let us assume that CS0 is not used in the design and the Debounce value for each button (CS1–CS8) is set as 3. The Button Scan Rate constant for such a design is 35 ms (see Table 5 on page 17), which results in a Button Scan Rate to be (35 + 391 ms) 426 ms.

The response time for such a design is given as:

$$RT_{CBT} = 35 + \left[35 \times \left\{Round_{down}\left((3 - 1)/3\right) + 1\right\}\right] = 70\ ms$$

$$RT_{FBT} = 426 + \left[35 \times \left\{Round_{down}\left((3 - 1)/3\right) + 1\right\}\right] = 461\ ms$$

Device Modes

The register map is divided into five modes.

- Operating mode
- LED Configuration mode
- Device Configuration mode
- Production Line Test mode
- Debug Data mode

The following sections give an overview of each mode. Each register mode consists of different sets of registers. Refer to the Appendix - Register Map section for description of all the registers in detail.

Operating Mode

The Host must use this mode after configuring the device in run time. The following can be configured in this mode:

1. Host control GPO logic levels
2. Deep Sleep mode entry
3. Software Reset
4. Device mode change

Host can read the following device information in this mode:

1. CapSense current and latched status
2. Current configuration (factory default or user configuration)
3. Flash checksum
4. RAM checksum
5. Device ID and firmware revision

LED Configuration Mode

The Host must use this mode to configure the device and revert back to the Operating mode after configuration.

The Host can configure the following in this mode:

1. Analog voltage output settings
2. Power-on LED effects
3. Button Touch LED effects
4. LED ON Time
5. Standby Mode LED brightness
6. Device Mode change

Device Configuration Mode

The Host must use this mode to configure the device and then revert back to operating mode after configuration is done. Host can configure the following in this mode:

1. I^2C address
2. FSS group buttons
3. Toggle ON/OFF option
4. Button Sensitivity, Debounce, Finger Threshold
5. Buzzer settings
6. Automatic threshold settings
7. Button Scan rate settings (power settings)
8. Noise Immunity settings
9. Button Auto Reset time
10. Design Optimization settings
11. Save settings to flash
12. Load factory default configuration
13. Device mode change

Production Line Test Mode

The Host must use this mode only during the design validation and production testing stage of product development.

The Host can configure the following in this mode:

1. Host-controlled GPO logic levels
2. Changing device mode

The Host can read the following device information in this mode, which helps in Production Line Test:

1. System Diagnostics data
   - Button short to ground
   - Button short to another button
   - Button short to V_{DD}
   - Button Parasitic capacitance > 40 pF
   - Improper value of C_{MOD} value connected
2. All buttons SNR values
3. Valid button count
4. CapSense current status

Debug Data Mode

The Host must use this mode only during the design validation stage of product development.

The Host can configure the following in this mode:

1. Host-controlled GPO logic levels
2. Parameter type and button number, which the host wants to debug
3. Changing device mode

The Host can read the following device information in this mode, which helps in design validation:

1. CapSense Raw data (Raw count, baseline and signal)
2. CapSense button SNR
3. Button parasitic capacitance
4. CapSense current status

Steps to Configure CY8CMBR2110

To configure the CY8CMBR2110, follow these steps:

1. Change Device mode to LED Configuration mode.
2. Wait for 55 ms.
3. Write to all the configuration registers in the LED Configuration mode.
4. Wait for 55 ms.
5. Change Device mode to Device Configuration mode.
6. Wait for 55 ms.
7. Write to all the configuration registers in the Device Configuration mode.
8. Calculate checksum and enter this value in the registers.

Checksum (Checksum_MSB (0x1E) and Checksum_LSB (0x1F) in the Device Configuration mode): Checksum is the sum of values of the registers (0x01–0x1F) in the LED Configuration mode and the registers (0x01–0x1D) in the Device Configuration mode. Checksum also takes the values of any reserved register bits. The host should not write to these bits and should add 0 for any such bit, while calculating checksum.

Checksum_Flash_xxx registers (in the Operating mode) indicate the checksum stored in the flash. Checksum_RAM_xxx registers (in the Operating mode) indicate the checksum calculated by the device and stored in the RAM.

9. Wait for 55 ms.
10. Read the Checksum matched bit in the Host_Mode register (in the Device Configuration mode) and verify that it is set to 1. If this bit is not set, start again from the first step and reconfigure the device. The host should keep a backup of the configuration data if this is needed.

Checksum matched bit: The CY8CMBR2110 calculates the checksum and compares that with the Checksum register value entered by the host. If both the values match, the Checksum matched bit in the Host_Mode register (in the Device Configuration mode) is set to 1. If the values do not match (indicating a possible I^2C write error) this bit is cleared to 0. The host can read the Checksum_RAM_xxx register (in the Operating mode) to know the device calculated checksum.

11. If the Checksum matched bit is set to 1, then set the Save to Flash bit in the Host_mode register.

Save to Flash bit: On a Save to Flash, the following sequence is executed:

- The device copies the 64-byte data (LED Configuration mode and Device Configuration mode) to the flash.
- A software reset is done.
- After software reset, the device is in Operating mode.

Any configuration changes are not applicable unless a Save to Flash is done, which is useful when the device has to be configured only once for all future operations. To ensure a flawless Save to Flash, the device power supply must be stable, with V_{DD} fluctuations limited to ±5% of the V_{DD}.

12. After a Save to Flash, wait for (T_{SAVE_FLASH} + Device initialization) time. T_{SAVE_FLASH} is mentioned in the Flash Write Time Specifications. The device initialization time is 350 ms (normal Noise Immunity) or 1000 ms (high Noise Immunity).
13. Read the Factory defaults loaded bit in Device_Stat register (in Operating mode).

Factory Defaults Loaded bit: After every reset, the device loads the RAM with the flash content and verifies the RAM checksum with the flash checksum to ensure there is no flash corruption. If the checksum differs, then the device identifies it as a flash corruption and loads the factory default value in the RAM, and sets the Factory Defaults Loaded bit. This resets any register value previously changed by the host. Factory default values of each register are mentioned in the Register Map.

If the factory defaults are loaded, the I^2C address of the device also changes from the current address (set by the host) to the default address, 37h. The host must then check for the default I^2C address on the I^2C bus to communicate with the CY8CMBR2110.

14. Setting the Factory Defaults Loaded bit corrupts the flash and the host needs to reconfigure the device from the first step. If this bit is clear, then the device is successfully configured.

CY8CMBR2110 Reset

You can reset the CY8CMBR2110 either through hardware or software using the following options:

- Hardware Reset: For this option, toggle power on the CY8CMBR2110 pins. There are two types of hardware reset:
  - Power reset – Turn OFF the external power supply on the device V_{DD} line and turn ON again (after power down, ensure that the V_{DD} is less than 100 mV, before powering backup). On a power reset, there is a high-going pulse of 16 ms on the HostControlGPO1 pin.
  - XRES reset – Pull the device XRES pin HIGH and then pull LOW. On an XRES reset, there is no pulse on HostControlGPO1 pin. In all other respects, XRES reset is identical to power reset.

On a hardware reset, the LED Configuration mode and Device Configuration mode register values are loaded from the flash to the RAM. All the device blocks are initialized, System Diagnostics is done, and an initial 5-ms pulse is sent on all the GPOx associated with any failing CSx. This is done within 350 ms (normal Noise Immunity) or 1000 ms (high Noise Immunity). Power-on LED Effects (if enabled) are then seen on all the remaining GPOs. After this, the device is in the Operating mode and normal operation begins.

- Software Reset: This is done by writing 1 to the Software Reset bit in the Host_Mode register (in Operating mode). On a software reset, the LED Configuration mode and Device Configuration mode register values are loaded from the flash to the RAM. The device auto-clears the Software Reset bit and all the device blocks are initialized. This is done within 350 ms (normal Noise Immunity) or 1000 ms (high Noise Immunity). After this, the device is in the Operating mode and normal operation begins. System Diagnostics is not done and Power-on LED Effects do not occur. If the user has configured the device for Power-on LED Effects and saved the settings to flash, a hardware reset must be done to see the Power-on LED Effects.

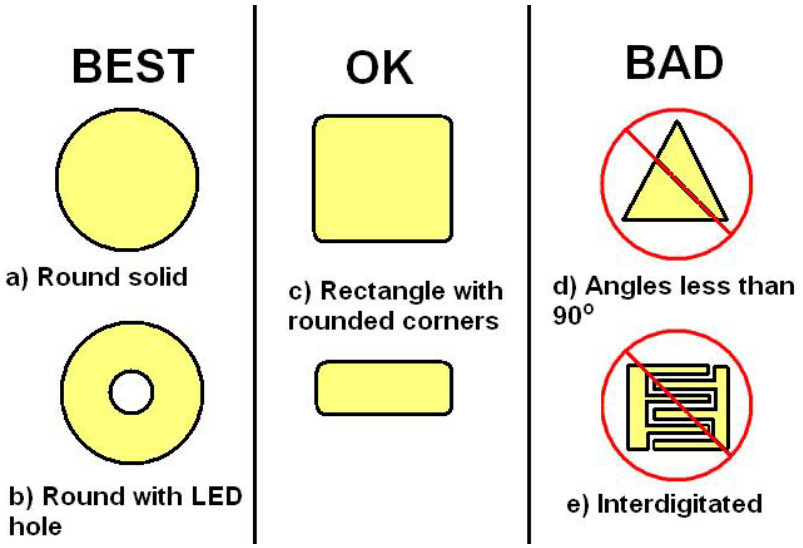
Layout Guidelines and Best Practices

Table 8. Layout Guidelines and Best Practices

Sl. No.	Category	Min	Max	Recommendations/Remarks
1	Button Shape	–	–	Solid round pattern, round with LED hole, rectangle with round corners
2	Button Size	5 mm	15 mm	Refer to the Design Toolbox
3	Button-Button spacing	Equal to Button Ground Clearance	–	8 mm (Y dimension in Figure 39 on page 26)
4	Button Ground Clearance	0.5 mm	2 mm	Refer to the Design Toolbox (X dimension in Figure 39 on page 26)
5	Ground Flood - Top layer	–	–	Hatched ground 7 mil trace and 45 mil grid (15% filling)
6	Ground Flood - Bottom layer	–	–	Hatched ground 7 mil trace and 70 mil grid (10% filling)
7	Trace Length from button pad to CapSense controller pins	–	450 mm	Refer to the Design Toolbox
8	Trace Width	0.17 mm	0.20 mm	0.17 mm (7 mil)
9	Trace Routing	–	–	Traces should be routed on the non-button side. If any non-CapSense trace crosses CapSense trace, ensure that intersection is orthogonal.
10	Via Position for the buttons	–	–	Via should be placed near the edge of the button to reduce trace length thereby increasing sensitivity
11	Via Hole Size for button traces	–	–	10 mil
12	No. of via on button trace	1	2	1
13	Distance of CapSense series resistor from button pin	–	10 mm	Place CapSense series resistors close to the device for noise suppression. Place CapSense resistors, which have highest priority, first.
14	Distance between any CapSense trace to ground Flood	10 mil	20 mil	20 mil
15	Device placement	–	–	Mount the Device on the layer opposite to button. The CapSense trace length between the Device and buttons should be minimum (see trace length above)
16	Placement of components in two layer PCB	–	–	Top Layer – buttons Bottom layer – device, other components and traces.
17	Placement of components in four layer PCB	–	–	Top Layer – buttons Second Layer – CapSense traces and V_{DD} (avoid V_{DD} traces below the buttons) Third Layer – hatched ground Bottom layer – CapSense controller, other components and non CapSense traces
18	Overlay thickness	0 mm	5 mm	Refer to the Design Toolbox
19	Overlay material	–	–	Should be non-conductive material. Glass, ABS Plastic, Formica, wood and so on. There should be no air gap between PCB and overlay. Use adhesive to stick the PCB and overlay.
20	Overlay adhesives	–	–	Adhesive should be non conductive and dielectrically homogenous. 467MP and 468MP adhesives made by 3M are recommended.
21	LED back lighting	–	–	Cut a hole in the button pad and use rear mountable LEDs. Refer to the PCB layout in the following section.
22	Board thickness	–	–	Standard board thickness for CapSense FR4 based designs is 1.6 mm.

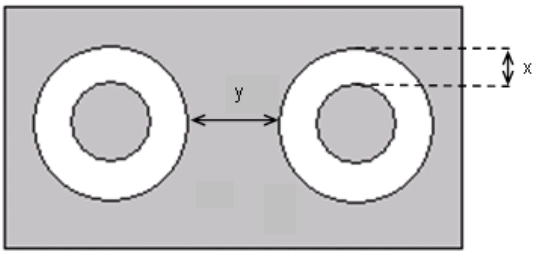
CapSense Button Shapes

Figure 38. CapSense Button Shapes



Button Layout Design

Figure 39. Button Layout Design

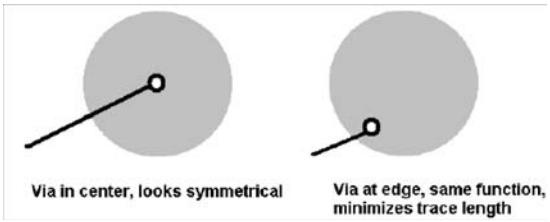


x: Button to ground clearance (Refer to Layout Guidelines and Best Practices on page 25)

y: Button to button clearance (Refer to Layout Guidelines and Best Practices on page 25)

Recommended via-hole Placement

Figure 40. Recommended via-hole Placement



Example PCB Layout Design with Ten CapSense Buttons and Ten LEDs

Figure 41. Top Layer

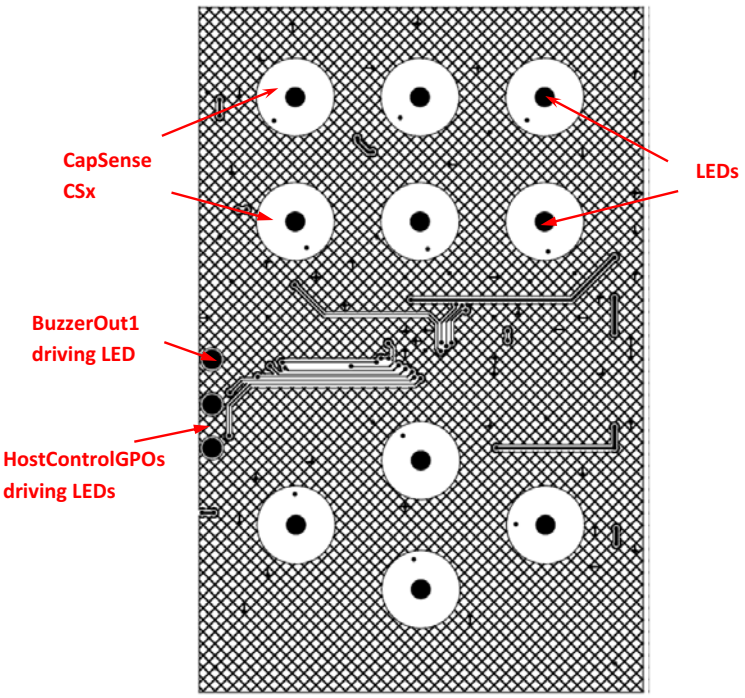
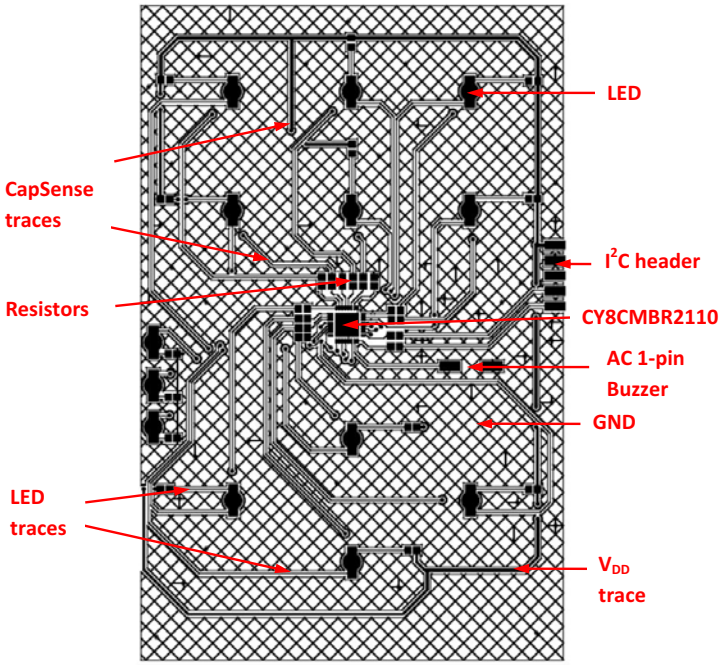


Figure 42. Bottom Layer



Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CMBR2110 device.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device.

Table 9. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Conditions
T_{STG}	Storage temperature	–55	+25	+125	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage at temperatures above 85 °C degrades reliability.
V_{DD}	Supply voltage relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC voltage on CapSense inputs and digital output pins	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIG}	Maximum current into any GPO pin	–25	–	+50	mA	
ESD	Electrostatic discharge voltage	2000	–	–	V	Human body model ESD
LU	Latch-up current	–	–	200	mA	In accordance with JESD78 standard

Operating Temperature

Table 10. Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_C	Commercial Temperature	0	–	+70	°C	
T_J	Operational Die Temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. Refer to Table 21 on page 35. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 11. DC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DD}[1],[2],[3]	Supply voltage	1.71	–	5.5	V	
I_{DD}	Supply current	–	3.4	4.0	mA	V_{DD} = 3.0 V, T_A = 25 °C
I_{DA}	Active current	–	3.4	4.0	mA	V_{DD} = 3.0 V, T_A = 25 °C, continuous button scan
I_{DS}	Deep sleep current	–	0.1	1.05	µA	V_{DD} = 3.0 V, T_A = 25 °C
I_{DL}	Low power sleep current	–	9.52	14.20	µA	V_{DD} = 3.0 V, T_A = 25 °C
I_{AV1}	Average current	–	90.5	–	µA	4 buttons used, 180 button touches per hour, average button touch time of 1000 ms, buzzer disabled, Button Touch LED Effects disabled, 10 pF < C_P of all buttons < 20 pF, Button Scan Rate = 541 ms, with power consumption optimized, Normal Noise Immunity level, Medium CSx sensitivity
I_{AV2}	Average current	–	111.2	–	µA	8 buttons used, 200 button touches per hour, average button touch time of 500 ms, buzzer disabled, average Button Touch LED Effects time of 1000 ms, 10 pF < C_P of all buttons < 20 pF, Button Scan Rate = 541 ms, with Response Time optimized, Normal Noise Immunity level, Medium CSx sensitivity
I_{AV3}	Average current	–	148.2	–	µA	10 buttons used, 200 button touches per hour, average button touch time of 500 ms, buzzer disabled, average Button Touch LED Effects time of 1000 ms, 10 pF < C_P of all buttons < 20 pF, Button Scan Rate = 362 ms, with Response Time optimized, Normal Noise Immunity level, Medium CSx sensitivity

Notes

8. When V_{DD} remains in the range of 1.75 V to 1.9 V for more than 50 µs, the slew rate (when moving from the 1.75 V to 1.9 V range to greater than 2 V) must be slower than 1 V/500 µs. This helps to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SRPOWER_UP parameter.
9. After power down, ensure that V_{DD} falls below 100 mV before powering back up
10. For proper CapSense block functionality, if the drop in V_{DD} exceeds 5% of the base V_{DD}, the rate at which V_{DD} drops should not exceed 200 mV/s. Base V_{DD} can be between 1.8 V and 5.5 V.

DC General Purpose I/O Specifications

These tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ T_A ≤ 85°C, 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 12. 3.0 V to 5.5 V DC General Purpose I/O Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH1}	High output voltage on GPO0–GPO9 (except GPO5)	V_{DD} – 0.20	–	–	V	I_{OH} ≤ 10 µA, maximum of 10-mA source current in all I/Os
V_{OH2}	High output voltage on GPO0–GPO9 (except GPO5)	V_{DD} – 0.90	–	–	V	I_{OH} = 1 mA, maximum of 20-mA source current in all I/Os
V_{OH3}	High output voltage on GPO5, BuzzerOut0, BuzzerOut1, HostControlGPO0, HostControlGPO1 pins	V_{DD} – 0.20	–	–	V	I_{OH} ≤ 10 µA, maximum of 10-mA source current in all I/Os
V_{OH4}	High output voltage on GPO5, BuzzerOut0, BuzzerOut1, HostControlGPO0, HostControlGPO1 pins	V_{DD} – 0.90	–	–	V	I_{OH} = 5 mA, maximum of 20 mA source current in all I/Os
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} > 3.3 V, maximum of 60-mA sink current on GPO0, GPO1 GPO2, GPO3, GPO4, BuzzerOut0, HostControlGPO0 pins and 60-mA sink current on GPO5, GPO6, GPO7, GPO8, GPO9, BuzzerOut1, HostControlGPO1 pins
V_{IL}	Input low voltage	–	–	0.80	V	
V_{IH}	Input high voltage	2.00	–	–	V	

Table 13. 2.4 V to 3.0 V DC General Purpose I/O Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH1}	High output voltage on GPO0–GPO9 (except GPO5)	V_{DD} – 0.20	–	–	V	I_{OH} ≤ 10 µA, maximum of 10-mA source current in all I/Os
V_{OH2}	High output voltage on GPO0–GPO9 (except GPO5)	V_{DD} – 0.40	–	–	V	I_{OH} = 0.2 mA, maximum of 10-mA source current in all I/Os
V_{OH3}	High output voltage on GPO5, BuzzerOut0, BuzzerOut1, HostControlGPO0, HostControlGPO1 pins	V_{DD} – 0.20	–	–	V	I_{OH} ≤ 10 µA, maximum of 10-mA source current in all I/Os
V_{OH4}	High output voltage on GPO5, BuzzerOut0, BuzzerOut1, HostControlGPO0, HostControlGPO1 pins	V_{DD} – 0.50	–	–	V	I_{OH} = 2 mA, maximum of 10-mA source current in all I/Os
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 10 mA, maximum of 30-mA sink current on GPO0, GPO1 GPO2, GPO3, GPO4, BuzzerOut0, HostControlGPO0 pins and 30 mA sink current on GPO5, GPO6, GPO7, GPO8, GPO9, BuzzerOut1, HostControlGPO1 pins
V_{IL}	Input low voltage	–	–	0.72	V	
V_{IH}	Input high voltage	1.40	–	–	V	

Table 14. 1.71 V to 2.4 V DC General Purpose I/O Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH1}	High output voltage on GPO0–GPO9 (except GPO5)	V_{DD} – 0.20	–	–	V	I_{OH} = 10 µA, maximum of 10-mA source current in all I/Os
V_{OH2}	High output voltage on GPO0–GPO9 (except GPO5)	V_{DD} – 0.50	–	–	V	I_{OH} = 0.5 mA, maximum of 10-mA source current in all I/Os
V_{OH3}	High output voltage on GPO5, BuzzerOut0, BuzzerOut1, HostControlGPO0, HostControlGPO1 pins	V_{DD} – 0.20	–	–	V	I_{OH} = 100 µA, maximum of 10-mA source current in all I/Os
V_{OH4}	High output voltage on GPO5, BuzzerOut0, BuzzerOut1, HostControlGPO0, HostControlGPO1 pins	V_{DD} – 0.50	–	–	V	I_{OH} = 2 mA, maximum of 10-mA source current in all I/Os
V_{OL}	Low output voltage	–	–	0.4	V	I_{OL} = 5 mA, maximum of 30-mA sink current on GPO0, GPO1 GPO2, GPO3, GPO4, BuzzerOut0, HostControlGPO0 pins and 20 mA sink current on GPO5, GPO6, GPO7, GPO8, GPO9, BuzzerOut1, HostControlGPO1 pins
V_{IL}	Input low voltage	–	–	0.3 x V_{DD}	V	
V_{IH}	Input high voltage	0.65 x V_{DD}	–	–	V	

DC I^2C Specifications

This table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ T_A ≤ 85°C, 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, & 1.71 V to 2.4 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 15. 3.0 V to 5.5 V DC General Purpose IO Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{ILI2C}	Input low level	–	–	0.25 x V_{DD}	V	3.1 V ≤ V_{DD} ≤ 5.5 V
		–	–	0.3 x V_{DD}	V	2.5 V ≤ V_{DD} ≤ 3.0 V
		–	–	0.3 x V_{DD}	V	1.71 V ≤ V_{DD} ≤ 2.4 V
V_{IHI2C}	Input high level	0.65 × V_{DD}	–	–	V	1.71 V ≤ V_{DD} ≤ 5.5 V

AC Electrical Specifications

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16. AC Chip-Level Specifications

Parameter	Description	Min	Max	Unit	Notes
SR_{POWER_UP}	Power supply slew rate	-	250	V/ms	V_{DD} slew rate during power up.
T_{XRST}	External reset pulse width at power-up	1		ms	Applicable after device power supply is active
T_{XRST2}	External reset pulse width after power-up	10		µs	Applicable after device V_{DD} has reached max value

AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 17. AC General Purpose I/O Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{Rise1}	Rise Time, Strong Mode on GPO0–GPO9 (except GPO5), Cload = 50 pF	15	–	80	ns	V_{DD} = 3.0 to 3.6 V, 10% to 90%
T_{Rise2}	Rise Time, Strong Mode on GPO5, BuzzerOut0, BuzzerOut1, HostControlGPO0, HostControlGPO1 pins, Cload = 50 pF	10	–	50	ns	V_{DD} = 3.0 to 3.6 V, 10% to 90%
T_{Rise3}	Rise Time, Strong Mode Low Supply on GPO0–GPO9 (except GPO5), Cload = 50 pF	15	–	80	ns	V_{DD} = 1.71 to 3.0 V, 10% to 90%
T_{Rise4}	Rise Time, Strong Mode Low Supply on GPO5, BuzzerOut0, BuzzerOut1, HostControlGPO0, HostControlGPO1 pins, Cload = 50 pF	10	–	80	ns	V_{DD} = 1.71 to 3.0 V, 10% to 90%
T_{Fall1}	Fall Time, Strong Mode, Cload = 50 pF on all GPOs, BuzzerOut pins, HostControlGPO pins	10	–	50	ns	V_{DD} = 3.0 to 3.6 V, 90% to 10%
T_{Fall2}	Fall Time, Strong Mode Low Supply, Cload = 50 pF on all GPOs, BuzzerOut pins, HostControlGPO pins	10	–	70	ns	V_{DD} = 1.71 to 3.0 V, 90% to 10%

Flash Write Time Specifications

Unless otherwise specified in the following table, all limits guaranteed for VDD = 5.0 V.

Table 18. Flash Write Time Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{SAVE_FLASH1}	Time taken to write to flash	–	45	120	ms	T_A = 0 °C–100 °C
T_{SAVE_FLASH2}	Time taken to write to flash	–	70	240	ms	T_A = –40 °C–0 °C

CapSense Specifications

Table 19. CapSense Specifications

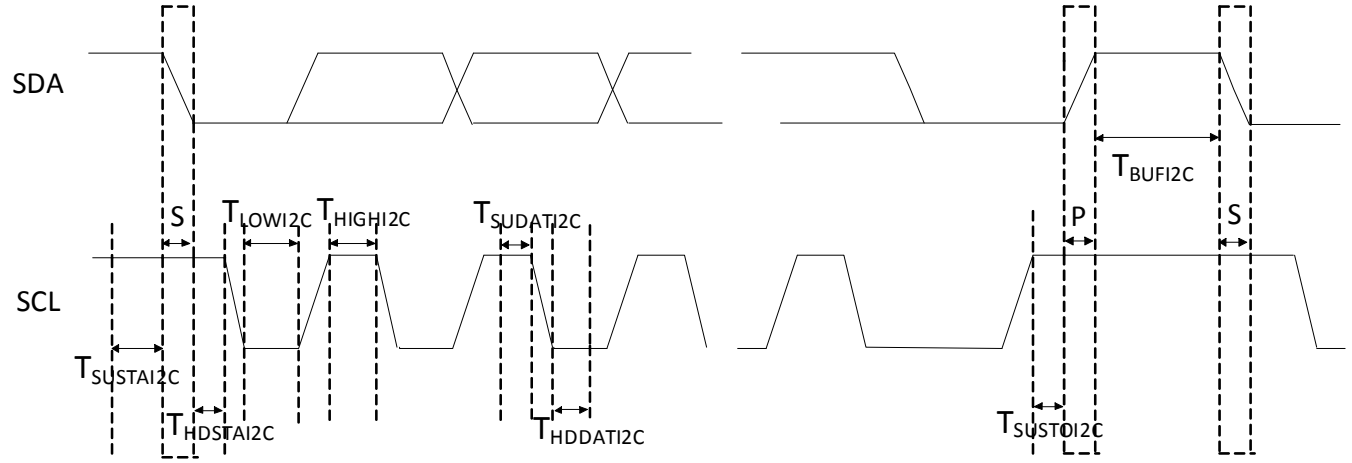
Parameter	Description	Min	Max	Unit	Notes
C_P	Parasitic capacitance	5.0	$(C_P+C_F)<40$[11]	pF	C_P is the total capacitance seen by the pin when no finger is present. C_P is sum of C_{BUTTON}, C_{TRACE}, and capacitance of the vias and C_{PIN}.
C_F	Finger capacitance	0.25	$(C_P+C_F)<40$[11]	pF	C_F is the capacitance added by the finger touch.
C_{PIN}	Capacitive load on pins as input	0.5	7	pF	
C_{MOD}	External modulating capacitor	2	2.4	nF	Mandatory for CapSense to work
R_S	Series resistor between pin and the button	–	616	Ω	Reduces the RF noise.

I²C Specifications

Table 20. I²C Specifications

Parameter	Description	Min	Max	Unit
F_{SCLI2C}	SCL clock frequency	0	100	kHz
$T_{SUSTAI2C}$	Setup time for a START condition	4.7	–	µs
$T_{HDSTAI2C}$	Hold time for a START condition. After this period, the first clock pulse is generated	4.0	–	µs
T_{LOWI2C}	LOW period of the SCL clock	4.7	–	µs
$T_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	µs
$T_{HDDATI2C}$	Data hold time	0	–	µs
$T_{SUDATI2C}$	Data setup time	250	–	ns
$T_{SUSTOI2C}$	Setup time for a STOP condition	4.0	–	µs
T_{BUFI2C}	Bus-free time between a STOP and START condition	4.7	–	µs

Figure 43. Definition of Timing on the I²C Bus



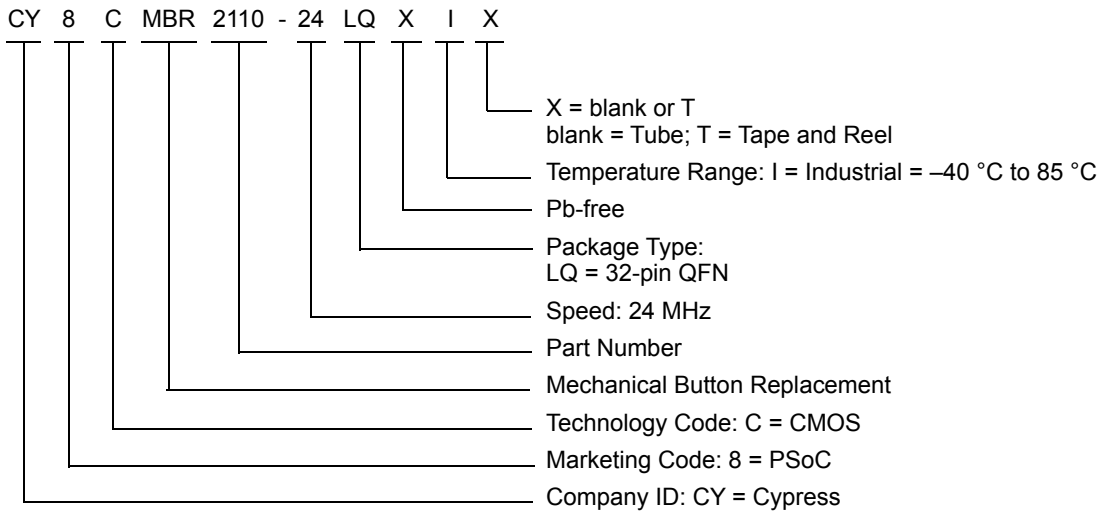
S – Start condition
P – Stop condition

Note
11. The max value of parasitic capacitance is 40 pF when the temperature is above 0 °C, and 38 pF at –45 °C.

Ordering Information

Ordering Code	Package Type	Operating Temperature	CapSense Inputs	GPO's	XRES Pin
CY8CMBR2110-24LQXI	32 Pad (5 × 5 × 0.6 mm) QFN	Industrial	10	10	Yes
CY8CMBR2110-24LQXIT	32 Pad (5 × 5 × 0.6 mm) QFN (tape and reel)	Industrial	10	10	Yes

Ordering Code Definitions



Package Information

Thermal Impedance

Table 21. Thermal Impedances per Package

Package	Typical θ_{JA} [12]
32-Pin QFN[13]	20 °C/W

Solder Reflow Specifications

Table 22 shows the solder reflow temperature limits that must not be exceeded.

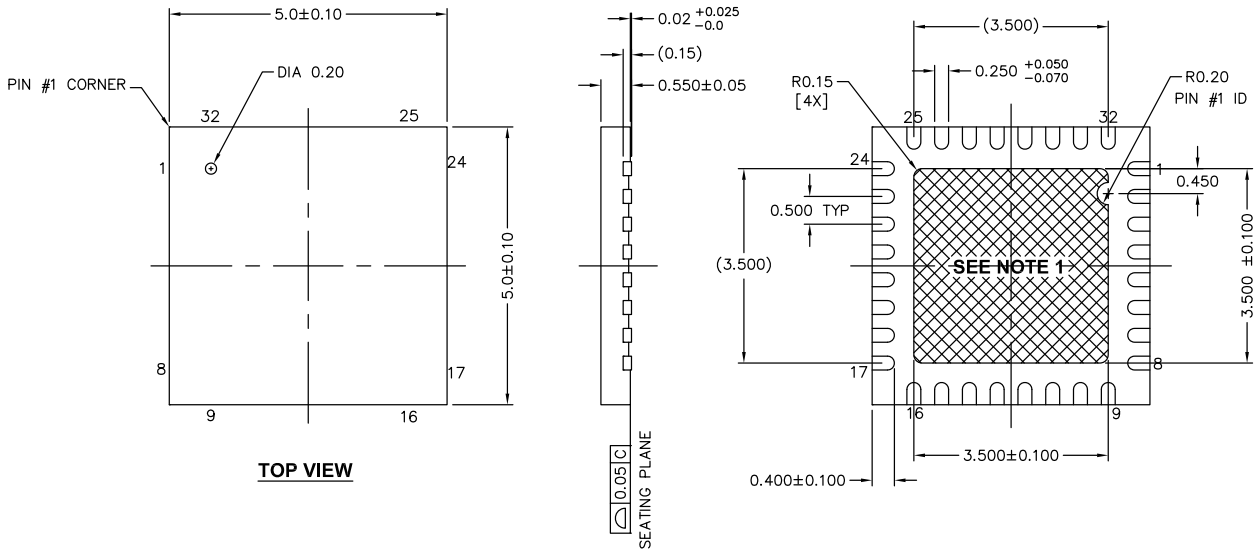
Table 22. Solder Reflow Specifications

Package	Minimum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
32-Pin QFN	260 °C	30 seconds

Notes
12. $T_J = T_A + Power \times \theta_{JA}$.
13. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

Package Diagram

Figure 44. 32-pin QFN (5 × 5 × 0.55 mm) LQ32 3.5 × 3.5 E-Pad (Sawn) Package Outline, 001-42168



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO−248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *E

Appendix - Register Map

1. Operating Mode

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Host Access[14]
Op,00h	HOST_MODE				Deep Sleep	Software Reset	Device_Mode[2:0]			RW:00
Op,01h	HOST_CONTROL_OUTPUT	Host Control GPO3	Host Control GPO2	Host Control GPO1	Host Control GPO0					RW:00
Op,02h	Reserved									#:??
Op,03h	DEVICE_STAT		Factory Defaults loaded							R:00
Op,04h	BUTTON_CURRENT_STAT0	CS7 Status	CS6 Status	CS5 Status	CS4 Status	CS3 Status	CS2 Status	CS1 Status	CS0 Status	R:00
Op,05h	BUTTON_CURRENT_STAT1							CS9 Status	CS8 Status	R:00
Op,06h	Reserved									#:??
Op,07h	BUTTON_LATCH_STAT0	CS7 latched	CS6 latched	CS5 latched	CS4 latched	CS3 latched	CS2 latched	CS1 latched	CS0 latched	R:00
Op,08h	BUTTON_LATCH_STAT1							CS9 latched	CS8 latched	R:00
Op,09h	Reserved									#:??
Op,0Ah	Reserved									#:??
Op,0Bh	Reserved									#:??
Op,0Ch	Reserved									#:??
Op,0Dh	Reserved									#:??
Op,0Eh	Reserved									#:??
Op,0Fh	Reserved									#:??
Op,10h	Reserved									#:??
Op,11h	Reserved									#:??
Op,12h	Reserved									#:??
Op,13h	Reserved									#:??
Op,14h	Reserved									#:??
Op,15h	Reserved									#:??
Op,16h	Reserved									#:??
Op,17h	Reserved									#:??
Op,18h	Reserved									#:??
Op,19h	Reserved									#:??
Op,1Ah	CS_FLASH_MSB	CheckSum_Flash_MSB[7:0]								R:00
Op,1Bh	CS_FLASH_LSB	CheckSum_Flash_LSB[7:0]								R:3B
Op,1Ch	CS_RAM_MSB	CheckSum_RAM_MSB[7:0]								R:00
Op,1Dh	CS_RAM_LSB	CheckSum_RAM_LSB[7:0]								R:3B
Op,1Eh	DEVICE_ID	Device_ID[7:0]								R:A1
Op,1Fh	FW_REV	Firmware_revision[7:0]								R:01

Note
14. Host Access is AB:XY
where:
AB = Read/Write access for the register
XY = Initial value of register on device power-on
For example:
RW:00 = The register is both Read/Write accessible, with initial value 00h.
R:A1 = The register is Read only, with initial value A1h.
#:?? = The register is reserved (no definite value stored)
The shaded areas represent reserved register bits.

1.1 HOST_MODE

Host Mode register

Individual Register Names and Addresses:

HOST_MODE: Op, 00h

	7	6	5	4	3	2	1	0
Access: FD				WC[15]: 0	WC[15]: 0	RW: 0		
Bit Name				Deep Sleep	Software Reset	Device Mode[2:0]		

This register is used to set the device into deep sleep mode, do device software reset, and set the device operation mode. To know more about Software reset, refer to CY8CMBR2110 Reset on page 24.

Bit	Name	Description
4	Deep Sleep	This bit decides the device Deep Sleep entry and is auto-cleared by the CapSense controller after the device exits from Deep Sleep. To know more about Deep Sleep, refer to Power Consumption and Operating Modes on page 21.
		0 Device is in normal sleep
		1 Initiate deep sleep mode
3	Software Reset	This bit resets the CapSense controller
		0 No impact
		1 Resets the CapSense controller
2:0	Device Mode	These bits decide the CapSense controller's device mode
		000 Operating mode
		001 LED configuration mode
		010 Device configuration mode
		011 Production line test mode
		100 Debug Data mode
		101 Not valid
		110 Not valid
		111 Not valid

Note
15. Device clears the Write Clear (WC) bit automatically after the required operation.

1.2 HOST_CONTROL_OUTPUT

Host Control Output register

Individual Register Names and Addresses:

HOST_CONTROL_OUTPUT: Op, 01h

	7	6	5	4	3	2	1	0
Access: FD	RW: 0							
Bit Name	Host Control GPO3	Host Control GPO2	Host Control GPO1	Host Control GPO0				

This register is used to control the logic levels of the Host Controlled GPOs. To know more, refer to Host Controlled GPOs on page 17.

Bit	Name	Description
7	Host Control GPO3	This bit controls the logic level of the host control GPO3
		0 Host control GPO3 is driven logic low
		1 Host control GPO3 is driven logic high
6	Host Control GPO2	This bit controls the logic level of the host control GPO2
		0 Host control GPO2 is driven logic low
		1 Host control GPO2 is driven logic high
5	Host Control GPO1	This bit controls the logic level of the host control GPO1
		0 Host control GPO1 is driven logic low
		1 Host control GPO1 is driven logic high
4	Host Control GPO0	This bit controls the logic level of the host control GPO0
		0 Host control GPO0 is driven logic low
		1 Host control GPO0 is driven logic high

1.3 DEVICE_STAT

Device Status register

Individual Register Names and Addresses:

DEVICE_STAT: Op, 03h

	7	6	5	4	3	2	1	0
Access: FD		R: 0						
Bit Name		Factory Defaults loaded						

This register is used to read whether the factory defaults or the user configuration is loaded at power-up.

Bit	Name	Description
6	Factory defaults loaded	This bit decides whether factory defaults or the user configuration is loaded at power up
		0 User configuration is loaded at power-up of device
		1 Factory default configuration is loaded at power-up of device

1.4 BUTTON_CURRENT_STATx

CapSense Button Current Status registers

Individual Register Names and Addresses:

BUTTON_CURRENT_STAT0: Op, 04h **BUTTON_CURRENT_STAT1: Op, 05h**

BUTTON_CURRENT_STAT0	7	6	5	4	3	2	1	0
Access: FD	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0
Bit Name	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0

BUTTON_CURRENT_STAT1	7	6	5	4	3	2	1	0
Access: FD							R: 0	R: 0
Bit Name							CS9	CS8

Reading from these registers gives the button ON/OFF status.

Bit	Name	Description
x	CSx	This bit gives the button ON/OFF status 0 Button OFF
		1 Button ON

1.5 BUTTON_LATCH_STATx

CapSense Button Latched Status registers

Individual Register Names and Addresses:

BUTTON_LATCH_STAT0: Op, 07h **BUTTON_LATCH_STAT1: Op, 08h**

BUTTON_LATCH_STAT0	7	6	5	4	3	2	1	0
Access: FD	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0
Bit Name	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0

BUTTON_LATCH_STAT1	7	6	5	4	3	2	1	0
Access: FD							R: 0	R: 0
Bit Name							CS9	CS8

Reading from these registers gives the button latched status.To know more about button latched status, refer to Latch Status Read on page 14.

1.6 CHECKSUM_FLASH_xxx

FLASH Settings Checksum registers

Individual Register Names and Addresses:

CHECKSUM_FLASH_MSB: Op, IAH **CHECKSUM_FLASH_LSB: Op, 1Bh**

CHECKSUM_FLASH_MSB	7	6	5	4	3	2	1	0
Access: FD	R: 00							
Bit Name	CheckSum_Flash_MSB[7:0]							

CHECKSUM_FLASH_LSB	7	6	5	4	3	2	1	0
Access: FD	R: 3Bh							
Bit Name	CheckSum_Flash_LSB[7:0]							

Reading 2 bytes from registers 1Ah, 1Bh gives the checksum of settings stored in the flash. Checksum is the sum of all the registers stored in flash for the Device Configuration (Reg 0x01-0x1D) and LED Configuration modes (Reg 0x01-0x1F). After the settings are saved to flash, the default settings change to the new value stored in flash.

1.7 CHECKSUM_RAM_xxx

RAM Settings Checksum registers

Individual Register Names and Addresses:

CHECKSUM_RAM_MSB: Op, 1Ch **CHECKSUM_RAM_LSB: Op, 1Dh**

CHECKSUM_RAM_MSB	7	6	5	4	3	2	1	0
Access: FD	R: 00							
Bit Name	CheckSum_RAM_MSB[7:0]							

CHECKSUM_RAM_LSB	7	6	5	4	3	2	1	0
Access: FD	R: 3Bh							
Bit Name	CheckSum_RAM_LSB[7:0]							

Reading 2 bytes from registers 1Ch, 1Dh gives the checksum of settings stored in the RAM. Checksum is the sum of all the registers in RAM for the Device Configuration (Reg 0x01-0x1D) and LED Configuration (Reg 0x01-0x1F) modes.

1.8 DEVICE_ID

Device Identity register

Individual Register Names and Addresses:

DEVICE_ID: Op, 1Eh

	7	6	5	4	3	2	1	0
Access: FD	R: A1							
Bit Name	Device ID[7:0]							

Reading 1 byte from this register gives the unique device ID through which the device can be identified. Device ID for this device is “0xA1”.

1.9 FW_REV

Firmware Revision register

Individual Register Names and Addresses:

FW_REV: Op, 1Fh

	7	6	5	4	3	2	1	0
Access: FD	R: 01							
Bit Name	Device ID[7:0]							

Reading 1 byte from this register gives the firmware revision.

2. LED Configuration Mode

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Host Access[16]
Lc,00h	HOST_MODE						Device_Mode[2:0]			RW:01
Lc,01h	LED_CONFIG	Last Button LED Effect Enable	Analog Voltage Output enable	Standby Mode LED Brightness [5:4]		LED ON Time enable	Button Touch LED Effects enable	Power On LED effects enable	Power On LED effect sequence	RW:00
Lc,02h	LED_FAD_PERIOD1	Period[7:0]								RW:00
Lc,03h	LED_FAD_PERIOD2	Period[7:0]								RW:00
Lc,04h	LED_FAD_PERIOD3	Period[7:0]								RW:00
Lc,05h	LED_FAD_PERIOD4	Period[7:0]								RW:00
Lc,06h	GPO000_LED_DIM_CONFIG1	Ramp_Up_Time[7:6]		High_Brightness[5:3]			LED_Scenario_Repeat[2:0]			RW:00
Lc,07h	GPO000_LED_DIM_CONFIG2	Ramp_Down_Time[7:6]		Low_Brightness[5:3]			Breathing effect	High_Time	Low_Time	RW:00
Lc,08h	GPO123_LED_DIM_CONFIG1	Ramp_Up_Time[7:6]		High_Brightness[5:3]			LED_Scenario_Repeat[2:0]			RW:00
Lc,09h	GPO123_LED_DIM_CONFIG2	Ramp_Down_Time[7:6]		Low_Brightness[5:3]			Breathing effect	High_Time	Low_Time	RW:00
Lc,0Ah	GPO456_LED_DIM_CONFIG1	Ramp_Up_Time[7:6]		High_Brightness[5:3]			LED_Scenario_Repeat[2:0]			RW:00
Lc,0Bh	GPO456_LED_DIM_CONFIG2	Ramp_Down_Time[7:6]		Low_Brightness[5:3]			Breathing effect	High_Time	Low_Time	RW:00
Lc,0Ch	GPO789_LED_DIM_CONFIG1	Ramp_Up_Time[7:6]		High_Brightness[5:3]			LED_Scenario_Repeat[2:0]			RW:00
Lc,0Dh	GPO789_LED_DIM_CONFIG2	Ramp_Down_Time[7:6]		Low_Brightness[5:3]			Breathing effect	High_Time	Low_Time	RW:00
Lc,0Eh	Reserved									#:??
Lc,0Fh	Reserved									#:??
Lc,10h	Reserved									#:??
Lc,11h	Reserved									#:??
Lc,12h	GPO000_PWRON_LED_DIM_CONFIG1	Ramp_Up_Time[7:6]		High_Brightness[5:3]			LED_Scenario_Repeat[2:0]			RW:00
Lc,13h	GPO000_PWRON_LED_DIM_CONFIG2	Ramp_Down_Time[7:6]		Low_Brightness[5:3]			High_Time[2:1]		Low_Time	RW:00
Lc,14h	GPO123_PWRON_LED_DIM_CONFIG1	Ramp_Up_Time[7:6]		High_Brightness[5:3]			LED_Scenario_Repeat[2:0]			RW:00
Lc,15h	GPO123_PWRON_LED_DIM_CONFIG2	Ramp_Down_Time[7:6]		Low_Brightness[5:3]			High_Time[2:1]		Low_Time	RW:00
Lc,16h	GPO456_PWRON_LED_DIM_CONFIG1	Ramp_Up_Time[7:6]		High_Brightness[5:3]			LED_Scenario_Repeat[2:0]			RW:00
Lc,17h	GPO456_PWRON_LED_DIM_CONFIG2	Ramp_Down_Time[7:6]		Low_Brightness[5:3]			High_Time[2:1]		Low_Time	RW:00
Lc,18h	GPO789_PWRON_LED_DIM_CONFIG1	Ramp_Up_Time[7:6]		High_Brightness[5:3]			LED_Scenario_Repeat[2:0]			RW:00
Lc,19h	GPO789_PWRON_LED_DIM_CONFIG2	Ramp_Down_Time[7:6]		Low_Brightness[5:3]			High_Time[2:1]		Low_Time	RW:00
Lc,1Ah	Reserved									#:??
Lc,1Bh	Reserved									#:??
Lc,1Ch	Reserved									#:??
Lc,1Dh	Reserved									#:??
Lc,1Eh	Reserved									#:??
Lc,1Fh	Reserved									#:??

Note
16. Host Access is AB:XY
where:
AB = Read/Write access for the register
XY = Initial value of register on device power-on
For example:
RW:00 = The register is both Read/Write accessible, with initial value 00h.
R:A1 = The register is Read only, with initial value A1h.
#:?? = The register is reserved (no definite value stored)
The shaded areas represent reserved register bits.

2.1 HOST_MODE

Host Mode register

Individual Register Names and Addresses:

HOST_MODE: Lc, 00h

	7	6	5	4	3	2	1	0
Access: FD						RW: 1		
Bit Name						Device Mode[2:0]		

This register is used to set the device operation mode.

Bit	Name	Description
2:0	Device Mode	These bits decide the CapSense controller device mode
		000 Operating mode
		001 LED configuration mode
		010 Device configuration mode
		011 Production line test mode
		100 Debug Data mode
		101 Not valid
		110 Not valid
		111 Not valid

2.2 LED_CONFIG

LED Effects Configuration register

Individual Register Names and Addresses:

LED_CONFIG: Lc, 01h

	7	6	5	4	3	2	1	0
Access: FD	RW: 0	RW: 0	RW: 0		RW: 0	RW: 0	RW: 0	RW: 0
Bit Name	Last Button LED Effect enable	Analog Voltage Output Enable	Standby Mode LED brightness[5:4]		LED On time Enable	Button Touch LED effects Enable	Power on LED effects enable	Power on LED effects Sequence

This register is used to enable/disable Button Touch LED Effects and Power-on LED Effects, and decides the power-on LED effect sequence, LED ON Time enable/disable, sets the Standby Mode LED Brightness, analog voltage output enable/disable, and Last Button LED Effect enable/disable.

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="3">7</td><td rowspan="3">Last Button LED Effect enable</td><td>This bit decides whether LED effects should continue on all the GPOs or only on the last button touched</td></tr>
<tr><td>0 LED effects on any button touched based on the settings</td></tr>
<tr><td>1 LED effects only on the last button touched</td></tr>
<tr><td rowspan="3">6</td><td rowspan="3">Analog Voltage Output enable</td><td>This bit decides whether Output pins can be used as open drain switches</td></tr>
<tr><td>0 Output pins cannot be used for Analog output voltage</td></tr>
<tr><td>1 Output pins can be used for Analog output voltage</td></tr>
<tr><td>5:4</td><td>Standby Mode LED Brightness</td><td>These bits set the Standby Mode LED brightness
<table>
<tr><th>Standby Mode LED Brightness Bits</th><th>LED Brightness</th></tr>
<tr><td>0b00</td><td>0%</td></tr>
<tr><td>0b01</td><td>20%</td></tr>
<tr><td>0b10</td><td>30%</td></tr>
<tr><td>0b11</td><td>50%</td></tr>
</table></td></tr>
<tr><td rowspan="3">3</td><td rowspan="3">LED On time Enable</td><td>This bit enables the LED ON time after button is released</td></tr>
<tr><td>0 LED ON time disabled</td></tr>
<tr><td>1 LED ON time enabled and LED ON time value is taken from the LED_FAD_PERIOD1 register.</td></tr>
<tr><td rowspan="3">2</td><td rowspan="3">Button Touch LED effects enable</td><td>This bit enables or disables the Button Touch LED effects. If this bit is not set, settings from register 0x06 – 0x0D are ignored.</td></tr>
<tr><td>0 Disable the Button Touch LED effects</td></tr>
<tr><td>1 Enable the Button Touch LED effects</td></tr>
<tr><td rowspan="3">1</td><td rowspan="3">Power on LED effects enable</td><td>This bit enables or disables the Power-on LED effects. If this bit is not set, settings from register 0x12 – 0x19 are ignored.</td></tr>
<tr><td>0 Disable the Power-on LED effects</td></tr>
<tr><td>1 Enable the Power-on LED effects</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">Power on LED effect sequence</td><td>This bit decides the Power-on LED Effects sequence on GPOs.
0 Power on LED effects on all GPOs appear concurrently</td></tr>
<tr><td>1 Power on LED effects on all GPOs appear sequentially. The sequence is GPO0>GPO1>.....GPO9</td></tr>
</table>

2.3 LED_FAD_PERIODx

LED Effects Global Timing registers

Individual Register Names and Addresses:

LED_FAD_PERIOD1: Lc, 02h **LED_FAD_PERIOD2: Lc, 03h**

LED_FAD_PERIOD3: Lc, 04h **LED_FAD_PERIOD4: Lc, 05h**

	7	6	5	4	3	2	1	0
Access: FD	RW: 00							
Bit Name	PERIOD[7:0]							

This register is used to set the LED effect timings. Each step increment in this register corresponds to increment of 20 ms in the LED effect timings.

2.4 GPOxxx_LED_DIM_CONFIG1

LED Effects configuration registers

Individual Register Names and Addresses:

GPO000_LED_DIM_CONFIG1:Lc,06h **GPO123_LED_DIM_CONFIG1:Lc,08h** **GPO456_LED_DIM_CONFIG1:Lc,0Ah**

GPO789_LED_DIM_CONFIG1:Lc,0Ch

	7	6	5	4	3	2	1	0
Access: FD	RW:00		RW: 00			RW: 00		
Bit Name	T_{RU}[7:6]		HIGH_BRIGHTNESS[5:3]			LED_SCENARIO_REPEAT[2:0]		

This register is used to set the ramp up time, high brightness intensity, and the LED scenario repeat rate for the LED effects. The following table gives the list of registers and the corresponding GPOs whose LED Effects are controlled by the register settings.

Register Name	GPOs with Defined Effect in the Register
GPO000_LED_DIM_CONFIG1	GPO0
GPO123_LED_DIM_CONFIG1	GPO1, GPO2, GPO3
GPO456_LED_DIM_CONFIG1	GPO4, GPO5, GPO6
GPO789_LED_DIM_CONFIG1	GPO7, GPO8, GPO9

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7:6</td><td>T_{RU}[7:6]</td><td>These bits decide the global setting time that will be used as ramp up time
<table>
<tr><th>T_{RU}[7:6]</th><th>Ramp Up Time</th></tr>
<tr><td>0b00</td><td>LED_FAD_PERIOD1</td></tr>
<tr><td>0b01</td><td>LED_FAD_PERIOD2</td></tr>
<tr><td>0b10</td><td>LED_FAD_PERIOD3</td></tr>
<tr><td>0b11</td><td>LED_FAD_PERIOD4</td></tr>
</table></td></tr>
<tr><td>5:3</td><td>HIGH_BRIGHTNESS[5:3]</td><td>These bits decide what should be the high brightness state intensity
<table>
<tr><th>HIGH_BRIGHTNESS[5:3]</th><th>Ramp Up Target Intensity</th></tr>
<tr><td>0b000</td><td>100%</td></tr>
<tr><td>0b001</td><td>90%</td></tr>
<tr><td>0b010</td><td>80%</td></tr>
<tr><td>0b011</td><td>65%</td></tr>
<tr><td>0b100</td><td>50%</td></tr>
<tr><td>0b101</td><td>40%</td></tr>
<tr><td>0b110</td><td>20%</td></tr>
<tr><td>0b111</td><td>0%</td></tr>
</table></td></tr>
<tr><td>2:0</td><td>LED_SCENARIO_REPEAT[2:0]</td><td>These bits decide how many times the LED effects should be repeated after the corresponding button is released.
<table>
<tr><th>LED_SCENARIO_REPEAT[2:0]</th><th>LED Scenario Repeat Rate</th></tr>
<tr><td>0b000</td><td>0</td></tr>
<tr><td>0b001</td><td>1</td></tr>
<tr><td>0b010</td><td>2</td></tr>
<tr><td>0b011</td><td>4</td></tr>
<tr><td>0b100</td><td>6</td></tr>
<tr><td>0b101</td><td>10</td></tr>
<tr><td>0b110</td><td>15</td></tr>
<tr><td>0b111</td><td>20</td></tr>
</table></td></tr>
</table>

2.5 GPOxxx_LED_DIM_CONFIG2

LED Effects configuration registers

Individual Register Names and Addresses:

GPO000_LED_DIM_CONFIG2:Lc, 07h **GPO123_LED_DIM_CONFIG2:Lc,09h** **GPO456_LED_DIM_CONFIG2:Lc,0Bh**
GPO789_LED_DIM_CONFIG2:Lc,0Dh

	7	6	5	4	3	2	1	0
Access: FD	RW: 00		RW: 00			RW: 0	RW: 0	RW: 0
Bit Name	T_{RD}[7:6]		LOW_BRIGHTNESS[5:3]			Breathing effect	T_H	T_L

These registers are used to set the ramp down time, low brightness intensity, the high brightness time, and the low brightness time for the LED effects. These registers also control the LED Breathing effect. The following table gives information about which GPO's LED effects are controlled by which register settings.

Register Name	GPOs with Defined Effect in the Register
GPO000_LED_DIM_CONFIG2	GPO0
GPO123_LED_DIM_CONFIG2	GPO1, GPO2, GPO3
GPO456_LED_DIM_CONFIG2	GPO4, GPO5, GPO6
GPO789_LED_DIM_CONFIG2	GPO7, GPO8, GPO9

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7:6</td><td>T_{RD}[7:6]</td><td>These bits decide the global setting time that will be used as ramp down time
<table>
<tr><th>T_{RD}[7:6]</th><th>Ramp Down Time</th></tr>
<tr><td>0b00</td><td>LED_FAD_PERIOD1</td></tr>
<tr><td>0b01</td><td>LED_FAD_PERIOD2</td></tr>
<tr><td>0b10</td><td>LED_FAD_PERIOD3</td></tr>
<tr><td>0b11</td><td>LED_FAD_PERIOD4</td></tr>
</table></td></tr>
<tr><td>5:3</td><td>LOW_BRIGHTNESS[5:3]</td><td>These bits decide what should be the low brightness state intensity
<table>
<tr><th>LOW_BRIGHTNESS[5:3]</th><th>Ramp Down Target Intensity</th></tr>
<tr><td>0b000</td><td>0%</td></tr>
<tr><td>0b001</td><td>10%</td></tr>
<tr><td>0b010</td><td>20%</td></tr>
<tr><td>0b011</td><td>30%</td></tr>
<tr><td>0b100</td><td>40%</td></tr>
<tr><td>0b101</td><td>60%</td></tr>
<tr><td>0b110</td><td>80%</td></tr>
<tr><td>0b111</td><td>100%</td></tr>
</table></td></tr>
<tr><td>2</td><td>Breathing effect</td><td>This bit decides whether LED effects should be repeated while the button is kept touched
0 LED effects are not repeated while the button is kept touched
1 LED effects are repeated while the button is kept touched</td></tr>
</table>

Bit	Name	Description
1	T_H	This bit decides the global setting time that will be used as high brightness time. T_H = 0: LED_FAD_PERIOD1 T_H = 1: LED_FAD_PERIOD2
0	T_L	This bit decides the global setting time that will be used as low brightness time. T_L = 0: LED_FAD_PERIOD1 T_L = 1: LED_FAD_PERIOD2

2.6 GPOxxx_PWRON_LED_DIM_CONFIG1

Power-on LED Effects configuration registers

Individual Register Names and Addresses:

GPO000_PWRON_LED_DIM_CONFIG1:Lc, 12h **GPO123_PWRON_LED_DIM_CONFIG1:Lc, 14h**
GPO456_PWRON_LED_DIM_CONFIG1:Lc, 16h **GPO789_PWRON_LED_DIM_CONFIG1:Lc, 18h**

	7	6	5	4	3	2	1	0
Access: FD	RW: 00		RW: 00			RW: 00		
Bit Name	T_{RU}[7:6]		HIGH_BRIGHTNESS[5:3]			LED_SCENARIO_REPEAT[2:0]		

These registers are used to set the ramp up time, high brightness intensity and the LED scenario repeat rate for Power-on LED Effects. The following table gives information about what GPO's power-on LED effects are controlled by which register settings.

Register Name	GPOs with Defined Effect in the Register
GPO000_PWRON_LED_DIM_CONFIG1	GPO0
GPO123_PWRON_LED_DIM_CONFIG1	GPO1, GPO2, GPO3
GPO456_PWRON_LED_DIM_CONFIG1	GPO4, GPO5, GPO6
GPO789_PWRON_LED_DIM_CONFIG1	GPO7, GPO8, GPO9

Bit	Name	Description
7:6	T_{RU}[7:6]	These bits decide the global setting time that will be used as ramp up time. T_{RU}[7:6] = 0b00: LED_FAD_PERIOD1 T_{RU}[7:6] = 0b01: LED_FAD_PERIOD2 T_{RU}[7:6] = 0b10: LED_FAD_PERIOD3 T_{RU}[7:6] = 0b11: LED_FAD_PERIOD4

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>5:3</td><td>HIGH_BRIGHTNESS[5:3]</td><td>These bits decide what should be the high brightness state intensity.
<table>
<tr><th>HIGH_BRIGHTNESS[5:3]</th><th>Ramp Up Target Intensity</th></tr>
<tr><td>0b000</td><td>100%</td></tr>
<tr><td>0b001</td><td>90%</td></tr>
<tr><td>0b010</td><td>80%</td></tr>
<tr><td>0b011</td><td>65%</td></tr>
<tr><td>0b100</td><td>50%</td></tr>
<tr><td>0b101</td><td>40%</td></tr>
<tr><td>0b110</td><td>20%</td></tr>
<tr><td>0b111</td><td>0%</td></tr>
</table></td></tr>
<tr><td>2:0</td><td>LED_SCENARIO_REPEAT[2:0]</td><td>These bits decide on how many times the Power-on LED effects should be repeated.
<table>
<tr><th>LED_SCENARIO_REPEAT[2:0]</th><th>LED Scenario Repeat Rate</th></tr>
<tr><td>0b000</td><td>0</td></tr>
<tr><td>0b001</td><td>1</td></tr>
<tr><td>0b010</td><td>2</td></tr>
<tr><td>0b011</td><td>4</td></tr>
<tr><td>0b100</td><td>6</td></tr>
<tr><td>0b101</td><td>10</td></tr>
<tr><td>0b110</td><td>15</td></tr>
<tr><td>0b111</td><td>20</td></tr>
</table></td></tr>
</table>

2.7 GPOxxx_PWRON_LED_DIM_CONFIG2

Power on LED Effects configuration registers

Individual Register Names and Addresses:

GPO000_PWRON_LED_DIM_CONFIG2:Lc, 13h **GPO123_PWRON_LED_DIM_CONFIG2:Lc, 15h**

GPO456_PWRON_LED_DIM_CONFIG2:Lc, 17h **GPO789_PWRON_LED_DIM_CONFIG2:Lc, 19h**

	7	6	5	4	3	2	1	0
Access: FD	RW: 00		RW: 00			RW: 00		RW: 0
Bit Name	T_{RD}[7:6]		LOW_BRIGHTNESS[5:3]			T_H[2:1]		T_L

These registers are used to set the ramp down time, low brightness intensity, the high brightness time, and the low brightness time in the power-on LED effect architecture. The following table gives information of what GPO's power-on LED effects are controlled by which register settings.

Register Name	GPOs with Defined Effect in the Register
GPO000_PWRON_LED_DIM_CONFIG2	GPO0
GPO123_PWRON_LED_DIM_CONFIG2	GPO1, GPO2, GPO3
GPO456_PWRON_LED_DIM_CONFIG2	GPO4, GPO5, GPO6
GPO789_PWRON_LED_DIM_CONFIG2	GPO7, GPO8, GPO9

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7:6</td><td>T_{RD}[7:6]</td><td>These bits decide which global setting time is used as ramp down time.
<table>
<tr><th>T_{RD}[7:6]</th><th>Ramp Down Time</th></tr>
<tr><td>0b00</td><td>LED_FAD_PERIOD1</td></tr>
<tr><td>0b01</td><td>LED_FAD_PERIOD2</td></tr>
<tr><td>0b10</td><td>LED_FAD_PERIOD3</td></tr>
<tr><td>0b11</td><td>LED_FAD_PERIOD4</td></tr>
</table></td></tr>
<tr><td>5:3</td><td>LOW_BRIGHTNESS[5:3]</td><td>These bits decide the low-brightness state intensity.
<table>
<tr><th>LOW_BRIGHTNESS[5:3]</th><th>Ramp Down Target Intensity</th></tr>
<tr><td>0b000</td><td>0%</td></tr>
<tr><td>0b001</td><td>10%</td></tr>
<tr><td>0b010</td><td>20%</td></tr>
<tr><td>0b011</td><td>30%</td></tr>
<tr><td>0b100</td><td>40%</td></tr>
<tr><td>0b101</td><td>60%</td></tr>
<tr><td>0b110</td><td>80%</td></tr>
<tr><td>0b111</td><td>100%</td></tr>
</table></td></tr>
<tr><td>2:1</td><td>T_H[2:1]</td><td>These bits decide which global setting time is used as high-brightness time.
<table>
<tr><th>T_H[2:1]</th><th>High Brightness Time</th></tr>
<tr><td>0b00</td><td>LED_FAD_PERIOD1</td></tr>
<tr><td>0b01</td><td>LED_FAD_PERIOD2</td></tr>
<tr><td>0b10</td><td>LED_FAD_PERIOD3</td></tr>
<tr><td>0b11</td><td>LED_FAD_PERIOD4</td></tr>
</table></td></tr>
<tr><td>0</td><td>T_L</td><td>This bit decides which global setting time is used as low-brightness time.
<table>
<tr><th>T_L</th><th>Low Brightness Time</th></tr>
<tr><td>0</td><td>LED_FAD_PERIOD1</td></tr>
<tr><td>1</td><td>LED_FAD_PERIOD2</td></tr>
</table></td></tr>
</table>

3. Device Configuration Mode

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Host Access[17]
Dc,00h	HOST_MODE			Load factory defaults	Checksum matched	Save to flash	Device_Mode[2:0]			RW:12
Dc,01h	I2C_CFG		I2C_Address[6:0]							RW:37
Dc,02h	DEV_FEATURES					Auto_reset[4:3]		Automatic Threshold	EMC	RW:02
Dc,03h	FSS_GROUP0	CS7_FSS	CS6_FSS	CS5_FSS	CS4_FSS	CS3_FSS	CS2_FSS	CS1_FSS	CS0_FSS	RW:00
Dc,04h	FSS_GROUP1							CS9_FSS	CS8_FSS	RW:00
Dc,05h	Reserved									#:??
Dc,06h	TOGGLE0	CS7_Toggle	CS6_Toggle	CS5_Toggle	CS4_Toggle	CS3_Toggle	CS2_Toggle	CS1_Toggle	CS0_Toggle	RW:00
Dc,07h	TOGGLE1							CS9_Toggle	CS8_Toggle	RW:00
Dc,08h	Reserved									#:??
Dc,09h	SENSITIVITY0	CS3_Sensitivity		CS2_Sensitivity		CS1_Sensitivity		CS0_Sensitivity		RW:00
Dc,0Ah	SENSITIVITY1	CS7_Sensitivity		CS6_Sensitivity		CS5_Sensitivity		CS4_Sensitivity		RW:00
Dc,0Bh	SENSITIVITY2					CS9_Sensitivity		CS8_Sensitivity		RW:00
Dc,0Ch	Reserved									#:??
Dc,0Dh	Reserved									#:??
Dc,0Eh	CS0_DEB	CS0_Debounce[7:0]								RW:01
Dc,0Fh	CS1-CS9_DEB	CS1-CS9_Debounce[7:0]								RW:01
Dc,10h	Reserved									#:??
Dc,11h	FINGER_THRESHOLD0	CS1_Finger_Threshold[7:4]				CS0_Finger_Threshold[3:0]				RW:00
Dc,12h	FINGER_THRESHOLD1	CS3_Finger_Threshold[7:4]				CS2_Finger_Threshold[3:0]				RW:00
Dc,13h	FINGER_THRESHOLD2	CS5_Finger_Threshold[7:4]				CS4_Finger_Threshold[3:0]				RW:00
Dc,14h	FINGER_THRESHOLD3	CS7_Finger_Threshold[7:4]				CS6_Finger_Threshold[3:0]				RW:00
Dc,15h	FINGER_THRESHOLD4	CS9_Finger_Threshold[7:4]				CS8_Finger_Threshold[3:0]				RW:00
Dc,16h	Reserved									#:??
Dc,17h	Reserved									#:??
Dc,18h	Reserved									#:??
Dc,19h	Reserved									#:??
Dc,1Ah	SCANRATE	Power consumption optimized	ScanRate[6:0]							RW:00
Dc,1Bh	BUZZER_CONFIG		Buzzer_Enable	Pins	Pin0 Idle State		Frequency[2:0]			RW:00
Dc,1Ch	BUZ_OP_DURATION		BuzzerDelay_Value[6:0]							RW:00
Dc,1Dh	CUSTOM_CFG1	Customer_Check_Data[7:0]								RW:00
Dc,1Eh	CHECKSUM_MSB	Checksum_MSB[7:0]								RW:00
Dc,1Fh	CHECKSUM_LSB	Checksum_LSB[7:0]								RW:3B

Note
17. Host Access is AB:XY
where:
AB = Read/Write access for the register
XY = Initial value of register on device power-on
For example:
RW:00 = The register is both Read/Write accessible, with initial value 00h.
R:A1 = The register is Read only, with initial value A1h.
#:?? = The register is reserved (no definite value stored)
The shaded areas represent reserved register bits

3.1 HOST_MODE

Host Mode register

Individual Register Names and Addresses:

HOST_MODE: Dc, 00h

	7	6	5	4	3	2	1	0
Access: FD			WC[18]: 0	R: 1	WC[18]: 0	RW: 2		
Bit Name			Load factory defaults	Checksum matched	Save to flash	Device Mode[2:0]		

This register is used to save the configuration to flash, decide the device operation mode, and load factory defaults. This register also tells whether the checksum is matched; to know more about Checksum match, refer to Steps to Configure CY8CMBR2110 on page 24.

Bit	Name	Description
5	Load factory defaults	This bit is used to load factory default setting in RAM. However user configured FLASH area does not get updated with these settings
		0 No impact
		1 Load factory defaults and bit is self cleared after loading factory defaults
4	Checksum matched	This bit is set or cleared based on the host sent checksum and the checksum calculated with the register data of device configuration mode and LED configuration mode
		0 Host sent checksum and checksum calculated did not match
		1 Host sent checksum and checksum calculated matched
3	Save to flash	This bit is used to store the current configuration into flash
		0 No impact
		1 stores the current configuration into flash
2:0	Device Mode	These bits decide the CapSense controller device mode
		000 Operating mode
		001 LED configuration mode
		010 Device configuration mode
		011 Production line test mode
		100 Debug Data mode
		101 Not valid
		110 Not valid
		111 Not valid

Note
18. Device clears the Write Clear (WC) bit automatically after the required operation.

3.2 I2C_CFG

I²C configuration register

Individual Register Names and Addresses:

I2C_CFG: Dc, 01h

	7	6	5	4	3	2	1	0
Access: FD		RW: 37						
Bit Name		I2C_Address[6:0]						

This register is used to set the I²C slave address. Slave address range is 0x00-0x7F.

Bit	Name	Description
6:0	I2C_Address[6:0]	These bits set the 7-bit I²C slave address

3.3 DEV_FEATURES

Device Features configuration register

Individual Register Names and Addresses:

DEV_FEATURES: Dc, 02h

	7	6	5	4	3	2	1	0
Access: FD					RW: 0		RW:1	RW:0
Bit Name					ARST_Delay[4:3]		Automatic Threshold	EMC

This register is used to enable/disable automatic thresholds and noise immunity level, and set the Button Auto Reset period.

Bit	Name	Description
3:2	ARST[3:2]	These bits decide Button Auto Reset period. ARST[3:2] / Button Auto Reset Period 0b00 – No limit 0b01 – No limit 0b10 – 5 sec 0b11 – 20 sec
1	Automatic Threshold	This bit decides whether all thresholds are automatically calculated (Automatic threshold enabled) or if the user should give finger threshold input and all other thresholds are calculated based on the finger threshold by the CapSense controller
		0 Disables automatic threshold calculation in SmartSense Auto-Tuning
		1 Enables automatic threshold calculation in SmartSense Auto-Tuning
0	EMC	This bit decides the noise immunity level
		0 Noise immunity level is normal
		1 Noise immunity level is high

3.4 FSS_GROUPx

CapSense FSS Group Setting registers

Individual Register Names and Addresses:

FSS_GROUP0: Dc, 03h **FSS_GROUP0: Dc, 04h**

FSS_GROUP0	7	6	5	4	3	2	1	0
Access: FD	RW: 0	RW: 0	RW: 0	RW: 0	RW: 0	RW: 0	RW: 0	RW: 0
Bit Name	CS7_FSS	CS6_FSS	CS5_FSS	CS4_FSS	CS3_FSS	CS2_FSS	CS1_FSS	CS0_FSS

FSS_GROUP1	7	6	5	4	3	2	1	0
Access: FD							RW: 0	RW: 0
Bit Name							CS9_FSS	CS8_FSS

These registers are used to set the buttons on which FSS needs to be applied.

Bit	Name	Description
x	CSx_FSS	This bit decides whether the button will be in the FSS group or not 0 Button not in FSS group
		1 Button in FSS group

3.5 TOGGLEx

Toggle Setting Registers

Individual Register Names and Addresses:

TOGGLE0: Dc, 06h **TOGGLE1: Dc, 07h**

TOGGLE0	7	6	5	4	3	2	1	0
Access: FD	RW: 0	RW: 0	RW: 0	RW: 0	RW: 0	RW: 0	RW: 0	RW: 0
Bit Name	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0

TOGGLE1	7	6	5	4	3	2	1	0
Access: FD							RW: 0	RW: 0
Bit Name							CS9	CS8

This register is used to decide if the CSx acts like a toggle switch.

Bit	Name	Description
x	CSx_FSS	This bit decides whether GPOx should be toggled based on CSx status or not 0 Toggle disabled
		1 Toggle enabled

3.6 SENSITIVITYx

CapSense Button Sensitivity Setting registers

Individual Register Names and Addresses:

SENSITIVITY0: Dc, 09h **SENSITIVITY1: Dc, 0Ah** **SENSITIVITY2: Dc, 0Bh**

SENSITIVITY0	7	6	5	4	3	2	1	0
Access: FD	RW: 0		RW: 0		RW: 0		RW: 0	
Bit Name	CS3_Sensitivity		CS2_Sensitivity		CS1_Sensitivity		CS0_Sensitivity	

SENSITIVITY1	7	6	5	4	3	2	1	0
Access: FD	RW: 0		RW: 0		RW: 0		RW: 0	
Bit Name	CS7_Sensitivity		CS6_Sensitivity		CS5_Sensitivity		CS4_Sensitivity	

SENSITIVITY2	7	6	5	4	3	2	1	0
Access: FD					RW: 0		RW: 0	
Bit Name					CS9_Sensitivity		CS8_Sensitivity	

These registers set the CapSense Button Sensitivity.

CSx_Sensitivity bits	Button Sensitivity
0b00	High Sensitivity
0b01	High Sensitivity
0b10	Medium Sensitivity
0b11	Low Sensitivity

3.7 CS0_DEB

CS0 Debounce Setting register

Individual Register Names and Addresses:

CS0_DEB: Dc, 0Eh

	7	6	5	4	3	2	1	0
Access: FD	RW: 01							
Bit Name	Debounce [7:0]							

This register sets the CS0 debounce. Range of this register is 1-255.

3.8 CS1-CS9_DEB

CS1 to CS9 Debounce Setting register

Individual Register Names and Addresses:

CS1-CS9_DEB: Dc, 0Fh

	7	6	5	4	3	2	1	0
Access: FD	RW: 01							
Bit Name	Debounce [7:0]							

This register sets the CS1 to CS9 buttons debounce. Range of this register is 1-255.

3.9 FINGER_THRESHOLDx

CapSense Button Finger Threshold Setting registers

Individual Register Names and Addresses:

FINGER_THRESHOLD0:Dc,11h FINGER_THRESHOLD1:Dc,12h FINGER_THRESHOLD2:Dc,13h
FINGER_THRESHOLD3:Dc,14h FINGER_THRESHOLD4:Dc,15h

FINGER_THRESHOLDx	7	6	5	4	3	2	1	0
Access: FD	RW: 00				RW: 00			
Bit Name	CSy_Finger_Threshold[7:4]				CSx_Finger_Threshold[3:0]			

These registers set the finger threshold of CapSense Buttons

Finger Threshold of Button ‘x’ = 50 + (13 * CSx_Finger_Threshold[3:0])

3.10 SCANRATE

Scan Rate Settings register

Individual Register Names and Addresses:

SCANRATE: Dc, 1Ah

	7	6	5	4	3	2	1	0
Access: FD	RW:00	RW:00						
Bit Name	Power consumption optimized	ScanRate[6:0]						

This register decides the Button Scan Rate based on the power consumption optimized bit, the number of buttons, and user configured scan rate. Based on the scan rate input selected in bits 6:0, one of the following offsets is added to the scan rate constant in the user configured scan rate mode.

0,6,12,20,29,39,49,61,73,86,99,114,128,144,160,176,194,211, 229,248,267,287,307,327,348,369,391,413,436,459,482,506

If Bit7 is set to '1' then power consumption optimization is enabled else response time optimization is enabled.

3.11 BUZZER_CONFIG

Buzzer Output Configuration register

Individual Register Names and Addresses:

BUZZER_CONFIG: Dc, 1Bh

	7	6	5	4	3	2	1	0
Access: FD		RW: 0	RW: 0	RW: 0		RW:00		
Bit Name		EN	PINS	IDLE0		Frequency[2:0]		

This register is used to enable buzzer output, select the number of buzzer output pins, buzzer output pins idle state logic level, and the buzzer output frequency

Bit	Name	Description
6	EN	This bit is used to enable or disable the buzzer output
		0 Disable the buzzer output
		1 Enable the buzzer output
5	PINS	This bit is used to select the number of buzzer output pins
		0 One buzzer output pin (AC 1-pin buzzer)
		1 Two buzzer output pins (AC 2-pin buzzer)
4	IDLE0	This bit decides the logic level of BuzzerOut0 in idle state
		0 BuzzerOut0 is driven logic'0' in idle state
		1 BuzzerOut0 is driven logic'1' in idle state
2:0	Frequency[2:0]	These bits decide the frequency of the buzzer output.

Frequency[2:0]	Buzzer Output Freq (KHZ)	Duty Cycle
0b000	4.00	50%
0b001	4.00	50%
0b010	2.67	66.7%
0b011	2.00	50%
0b100	1.60	60%
0b101	1.33	50%
0b110	1.14	57.1%
0b111	1.00	50%

3.12 BUZ_OP_DURATION

Buzzer Output Duration register

Individual Register Names and Addresses:

BUZ_OP_DURATION: Dc, 1Ch

	7	6	5	4	3	2	1	0
Access: FD		RW: 00						
Bit Name		BuzzerDelay_Values[6:0]						

The buzzer output is driven for the BuzzerDelay_Values[6:0] x Button Scan Rate constant. BuzzerDelay_Values can range from 1 to 127 if the buzzer is enabled. For the Button Scan Rate constant, see Table 7 on page 21.

3.13 CUSTOM_CONFIG1

Host Custom Data Storage registers

Individual Register Names and Addresses:

CUSTOM_CONFIG1: Dc, 1Dh

	7	6	5	4	3	2	1	0
Access: FD	RW: 0							
Bit Name	DATA[7:0]							

This register can be used by customers to write their own data and save to flash.

3.14 CHECKSUM_xxx

Device Configuration Checksum registers

Individual Register Names and Addresses:

CHECKSUM_MSB: Dc, 1Eh **CHECKSUM_LSB: Dc, 1Fh**

CHECKSUM_MSB	7	6	5	4	3	2	1	0
Access: FD	RW: 00							
Bit Name	CheckSum_MSB[7:0]							

CHECKSUM_LSB	7	6	5	4	3	2	1	0
Access: FD	RW: 3Bh							
BitName	CheckSum_LSB[7:0]							

Checksum is addition of register values from 0x01- 0x1F in LED configuration mode, and 0x01-0x1D in the Device configuration mode.

4. Production Line Testing Mode

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Host Access[19]
PI,00h	HOST_MODE	Host Control GPO3	Host Control GPO2	Host Control GPO1	Host Control GPO0		Device_Mode[2:0]			RW:03
PI,01h	Reserved									#:??
PI,02h	Reserved									#:??
PI,03h	BUTTON_COUNT					Number of working buttons detected				R:00
PI,04h	BUTTON_CURRENT_STAT0	CS7 Status	CS6 Status	CS5 Status	CS4 Status	CS3 Status	CS2 Status	CS1 Status	CS0 Status	R:00
PI,05h	BUTTON_CURRENT_STAT1							CS9 Status	CS8 Status	R:00
PI,06h	Reserved									#:??
PI,07h	CSx_SHORT_GND0	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0	R:00
PI,08h	CSx_SHORT_GND1							CS9	CS8	R:00
PI,09h	Reserved									#:??
PI,0Ah	CSx_SHORT_CSy0	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0	R:00
PI,0Bh	CSx_SHORT_CSy1							CS9	CS8	R:00
PI,0Ch	Reserved									#:??
PI,0Dh	CSx_CP_>40pF_0	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0	R:00
PI,0Eh	CSx_CP_>40pF_0							CS9	CS8	R:00
PI,0Fh	Reserved									#:??
PI,10h	CSx_SHORT_VDD0	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0	R:00
PI,11h	CSx_SHORT_VDD1							CS9	CS8	R:00
PI,12h	Reserved									#:??
PI,13h	CMOD_VALUE							C_{MOD} < 1 nF	C_{MOD} > 4 nF	R:00
PI,14h	CS01_SNR	CS1_SNR[3:0]				CS0_SNR[3:0]				R:00
PI,15h	CS23_SNR	CS3_SNR[3:0]				CS2_SNR[3:0]				R:00
PI,16h	CS45_SNR	CS5_SNR[3:0]				CS4_SNR[3:0]				R:00
PI,17h	CS67_SNR	CS7_SNR[3:0]				CS6_SNR[3:0]				R:00
PI,18h	CS89_SNR	CS9_SNR[3:0]				CS8_SNR[3:0]				R:00
PI,19h	Reserved									#:??
PI,1Ah	Reserved									#:??
PI,1Bh	Reserved									#:??
PI,1Ch	Reserved									#:??
PI,1Dh	Reserved									#:??
PI,1Eh	Reserved									#:??
PI,1Fh	Reserved									#:??

Note

19. Host Access is AB:XY
    where:
    AB = Read/Write access for the register
    XY = Initial value of register on device power-on
    For example:
    RW:00 = The register is both Read/Write accessible, with initial value 00h.
    R:A1 = The register is Read only, with initial value A1h.
    #:?? = The register is reserved (no definite value stored)
    The shaded areas represent reserved register bits

4.1 HOST_MODE

Host Mode register

Individual Register Names and Addresses:

HOST_MODE: PI, 00h

	7	6	5	4	3	2	1	0
Access: FD	RW: 0	RW: 0	RW: 0	RW: 0		RW: 3		
Bit Name	Host Control GPO3	Host Control GPO2	Host Control GPO1	Host Control GPO0		Device Mode[2:0]		

This register is used to control the logic levels of the host control GPOs, and decides the device operating mode.

Bit	Name	Description
7	Host Control GPO3	This bit controls the logic level of the host control GPO3
		0 Host control GPO3 is driven logic low
		1 Host control GPO3 is driven logic high
6	Host Control GPO2	This bit controls the logic level of the host control GPO2
		0 Host control GPO2 is driven logic low
		1 Host control GPO2 is driven logic high
5	Host Control GPO1	This bit controls the logic level of the host control GPO1
		0 Host control GPO1 is driven logic low
		1 Host control GPO1 is driven logic high
4	Host Control GPO0	This bit controls the logic level of the host control GPO0
		0 Host control GPO0 is driven logic low
		1 Host control GPO0 is driven logic high
2:0	Device Mode	These bits decide the CapSense controller device mode
		000 Operating mode
		001 LED configuration mode
		010 Device configuration mode
		011 Production line test mode
		100 Debug Data mode
		101 Not valid
		110 Not valid
		111 Not valid

4.2 BUTTON_COUNT

Detected Button Count register

Individual Register Names and Addresses:

BUTTON_COUNT: PI, 03h

	7	6	5	4	3	2	1	0
Access: FD					R: 0			
Bit Name					Working_Buttons [3:0]			

This register gives information about the number of working buttons detected. The Host can read this register and if the working button matches the host estimated count, then the System Diagnostics of all buttons has passed. If System Diagnostics of any button fails, then the button is disabled.

Bit	Name	Description
3:0	Working buttons	These bits contain the number of working buttons detected and can be read by the host to detect whether System Diagnostics passes or fails.

4.3 BUTTON_CURRENT_STATx

CapSense Button Current Status registers

Individual Register Names and Addresses:

BUTTON_CURRENT_STAT0: PI, 04h **BUTTON_CURRENT_STAT1: PI, 05h**

BUTTON_CURRENT_STAT0	7	6	5	4	3	2	1	0
Access: FD	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0
Bit Name	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0

BUTTON_CURRENT_STAT1	7	6	5	4	3	2	1	0
Access: FD							R: 0	R: 0
Bit Name							CS9	CS8

Reading from these registers gives the button ON/OFF status.

Bit	Name	Description
x	CSx	This bit gives the button ON/OFF status 0 Button OFF
		1 Button ON

4.4 CSx_SHORT_GNDx

CapSense Buttons Short to Ground Information registers

Individual Register Names and Addresses:

CSx_SHORT_GND0: PI, 07h **CSx_SHORT_GND1: PI, 08h**

CSx_SHORT_GND0	7	6	5	4	3	2	1	0
Access: FD	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0
Bit Name	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0

CSx_SHORT_GND1	7	6	5	4	3	2	1	0
Access: FD							R: 0	R: 0
Bit Name							CS9	CS8

This register gives information of any button that is shorted to ground. If any bit in the register is set to '1', then the corresponding button is connected to ground. CapSense buttons do not operate when they are connected to ground; these buttons are disabled.

4.5 CSx_SHORT_CSyz

CapSense Buttons Short to Other CapSense Button Information registers

Individual Register Names and Addresses:

CSx_SHORT_CSy0: PI, 0Ah **CSx_SHORT_CSy1: PI, 0Bh**

CSx_SHORT_CSy0	7	6	5	4	3	2	1	0
Access: FD	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0
Bit Name	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0

CSx_SHORT_CSy1	7	6	5	4	3	2	1	0
Access: FD							R: 0	R: 0
Bit Name							CS9	CS8

This register gives information of any button that is shorted to another button. If any two buttons are shorted to each other, then bits corresponding to both the buttons are set to '1' and the corresponding buttons are disabled.

4.6 CSx_CP_>40 pF_x

CapSense Buttons Parasitic Capacitance >40 pF Information registers

Individual Register Names and Addresses:

CSx_CP_>40 pF_0: PI, 0Dh **CSx_CP_>40 pF_1: PI, 0Eh**

CSx_CP_>40 pF_0	7	6	5	4	3	2	1	0
Access: FD	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0
Bit Name	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0

CSx_CP_>40 pF_1	7	6	5	4	3	2	1	0
Access: FD							R: 0	R: 0
Bit Name							CS9	CS8

This register gives information of buttons whose parasitic capacitance (C_P) is >40 pF. If any button C_P is >40 pF, then the bit in the register is set and that button is disabled.

4.7 CSx_SHORT_VDDx

CapSense Buttons Short to V_{DD} Information registers

Individual Register Names and Addresses:

CSx_SHORT_VDD0: PI, 10h **CSx_SHORT_VDD1: PI, 11h**

CSx_SHORT_VDD0	7	6	5	4	3	2	1	0
Access: FD	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0
Bit Name	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0

CSx_SHORT_VDD1	7	6	5	4	3	2	1	0
Access: FD							R: 0	R: 0
Bit Name							CS9	CS8

This register gives information of any button that is shorted to V_{DD}. If any bit in the register is set to '1', then the corresponding button is connected to V_{DD}. CapSense buttons do not operate when they are connected to V_{DD}, and are disabled.

4.8 CMOD_VALUE

Incorrect C_{MOD} Value Information registers

Individual Register Names and Addresses:

CMOD_VALUE: PI, 13h

	7	6	5	4	3	2	1	0
Access: FD							R: 0	R: 0
Bit Name							C_{MOD} < 1 nF	C_{MOD} > 4 nF

This register gives information if an incorrect value of C_{MOD} is connected. If the proper value of C_{MOD} is connected, then both bits ‘0’ and ‘1’ are set to ‘0’.

Bit	Name	Description
0	C_{MOD} > 4 nF	This bit gives information if C_{MOD} value detected is greater than the recommended range
		0 C_{MOD} is < 4 nF
		1 C_{MOD} is > 4 nF
1	C_{MOD} < 1 nF	This bit gives information if the C_{MOD} value detected is less than the recommended range
		0 C_{MOD} is > 1 nF
		1 C_{MOD} is < 1 nF

4.9 CSxy_SNR

CapSense Button SNR Information registers

Individual Register Names and Addresses:

CS01_SNR: PI, 14h **CS23_SNR: PI, 15h** **CS45_SNR: PI, 16h**
CS67_SNR: PI, 17h **CS89_SNR: PI, 18h**

	7	6	5	4	3	2	1	0
Access: FD	RW: 00				RW: 00			
Bit Name	CSy_SNR[7:4]				CSx_SNR[3:0]			

These registers give the signal to noise ratio information of the enabled buttons.

5. Debug Data Mode

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Host Access[20]
Dd,00h	HOST_MODE	Host Control GPO3	Host Control GPO2	Host Control GPO1	Host Control GPO0		Device_Mode[2:0]			RW:04
Dd,01h	BUTTON_NUMBER				Sensor[4:0]					RW:00
Dd,02h	PARAMETER				Parameter[4:0]					RW:00
Dd,03h	Reserved									R:00
Dd,04h	BUTTON_CURRENT_STAT0	CS7 Status	CS6 Status	CS5 Status	CS4 Status	CS3 Status	CS2 Status	CS1 Status	CS0 Status	R:00
Dd,05h	BUTTON_CURRENT_STAT1							CS9 Status	CS8 Status	R:00
Dd,06h	Reserved									#:??
Dd,07h	READ0	Data[7:0]								R:??
Dd,08h	READ1	Data[7:0]								R:??
Dd,09h	READ2	Data[7:0]								R:??
Dd,0Ah	READ3	Data[7:0]								R:??
Dd,0Bh	READ4	Data[7:0]								R:??
Dd,0Ch	READ5	Data[7:0]								R:??
Dd,0Dh	READ6	Data[7:0]								R:??
Dd,0Eh	READ7	Data[7:0]								R:??
Dd,0Fh	READ8	Data[7:0]								R:??
Dd,10h	READ9	Data[7:0]								R:??
Dd,11h	READ10	Data[7:0]								R:??
Dd,12h	READ11	Data[7:0]								R:??
Dd,13h	READ12	Data[7:0]								R:??
Dd,14h	READ13	Data[7:0]								R:??
Dd,15h	READ14	Data[7:0]								R:??
Dd,16h	READ15	Data[7:0]								R:??
Dd,17h	READ16	Data[7:0]								R:??
Dd,18h	READ17	Data[7:0]								R:??
Dd,19h	READ18	Data[7:0]								R:??
Dd,1Ah	READ19	Data[7:0]								R:??
Dd,1Bh	READ20	Data[7:0]								R:??
Dd,1Ch	READ21	Data[7:0]								R:??
Dd,1Dh	READ22	Data[7:0]								R:??
Dd,1Eh	READ23	Data[7:0]								R:??
Dd,1Fh	READ24	Data[7:0]								R:??

Note
20. Host Access is AB:XY
where:
AB = Read/Write access for the register
XY = Initial value of register on device power-on
For example:
RW:00 = The register is both Read/Write accessible, with initial value 00h.
R:A1 = The register is Read only, with initial value A1h.
#:?? = The register is reserved (no definite value stored)
The shaded areas represent reserved register bits.

5.1 HOST_MODE

Host Mode register

Individual Register Names and Addresses:

HOST_MODE: Dd, 00h

	7	6	5	4	3	2	1	0
Access: FD	RW: 0	RW: 0	RW: 0	RW: 0		RW: 4		
Bit Name	Host Control GPO3	Host Control GPO2	Host Control GPO1	Host Control GPO0		Device Mode[2:0]		

This register is used to control the logic levels of the host control GPOs, and decide the device operating mode.

Bit	Name	Description
7	Host Control GPO3	This bit controls the logic level of the host control GPO3
		0 Host control GPO3 is driven logic low
		1 Host control GPO3 is driven logic high
6	Host Control GPO2	This bit controls the logic level of the host control GPO2
		0 Host control GPO2 is driven logic low
		1 Host control GPO2 is driven logic high
5	Host Control GPO1	This bit controls the logic level of the host control GPO1
		0 Host control GPO1 is driven logic low
		1 Host control GPO1 is driven logic high
4	Host Control GPO0	This bit controls the logic level of the host control GPO0
		0 Host control GPO0 is driven logic low
		1 Host control GPO0 is driven logic high
2:0	Device Mode	These bits decide the CapSense controller device mode
		000 Operating mode
		001 LED configuration mode
		010 Device configuration mode
		011 Production line test mode
		100 Debug Data mode
		101 Not valid
		110 Not valid
		111 Not valid

5.2 BUTTON_NUMBER

Start Button Number of Debug Data register

Individual Register Names and Addresses:

BUTTON_NUMBER: Dd, 01h

	7	6	5	4	3	2	1	0
Access: FD					RW: 00			
Bit Name					Button[4:0]			

This register decides the start button number from which the data in registers 0x07-0x1F are filled. For example, if the button number is selected to '4' and the parameter (register no 0x02) is selected to raw count, then from register 0x07 raw count of buttons CS4, CS5, CS6, CS7, CS8, and CS9 are filled (assumption is all buttons are enabled).

5.3 PARAMETER

Parameter of Debug Data register

Individual Register Names and Addresses:

PARAMETER: Dd, 02h

	7	6	5	4	3	2	1	0
Access: FD						RW: 00		
Bit Name						Parameter[2:0]		

This register decides the type of data that is filled from register 0x07. For example, if the button number is selected to '4' and the parameter (register no 0x02) is selected to raw count, then from register 0x07 the raw count of buttons CS4, CS5, CS6, CS7, CS8, and CS9 are filled (the assumption is all buttons are enabled).

Parameter[2:0]	Parameter	Bytes Taken for Each Button
0	C_P	1
1	Raw Counts (RC)	2
2	Difference Counts (Dif)	2
3	Raw Counts (RC), Base Line (BL)	2 + 2 = 4
4	All parameters of one button (RC, BL, DIF, C_P, SNR)	2 + 2 + 2 + 1 + 1 = 8

For example, if the button number (register number 0x01) is selected to ‘3’ and parameter is selected to Dif, then the Difference counts of the buttons CS3, CS4, CS5, CS6, CS7, CS8, and CS9 (assuming all the buttons are enabled) are filled sequentially from register 0x07 to 0x14 with MSB filled first, followed by LSB (since Dif data is of two bytes for each button). The following table shows how the registers are filled in this case.

Register	Register Name	Value Written to Register
0x07	Read0	DIF3_MSB
0x08	Read1	DIF3_LSB
0x09	Read2	DIF4_MSB
0x0A	Read3	DIF4_LSB
0x0B	Read4	DIF5_MSB
0x0C	Read5	DIF5_LSB
0x0D	Read6	DIF6_MSB
0x0E	Read7	DIF6_LSB
0x0F	Read8	DIF7_MSB

Register	Register Name	Value Written to Register
0x10	Read9	DIF7_LSB
0x11	Read10	DIF8_MSB
0x12	Read11	DIF8_LSB
0x13	Read12	DIF9_MSB
0x14	Read13	DIF9_LSB

There are 25 debug data read registers (0x07-0x1F). Hence, 25 bytes of space is available for one single read. Therefore, if the parameter 3 is selected, the Raw Count and Baseline data of a maximum of six buttons can be read at a time. If there are ten buttons enabled in the design, then the host needs to read CS0 - CS5 first, and then change the button number (register number 0x01) to '6' and read CS6 - CS9 information.

If parameter 4 is selected, all the parameters (Raw Count, Baseline, Difference Count, Parasitic Capacitance, and SNR) of the selected button (from register 0x01) are written sequentially into the debug data read registers.

5.4 BUTTON_CURRENT_STATx

CapSense Button Current status registers

Individual Register Names and Addresses:

BUTTON_CURRENT_STAT0: Dd, 04h **BUTTON_CURRENT_STAT1: Dd, 05h**

BUTTON_CURRENT_STAT0	7	6	5	4	3	2	1	0
Access: FD	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0	R: 0
Bit Name	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0

BUTTON_CURRENT_STAT1	7	6	5	4	3	2	1	0
Access: FD							R: 0	R: 0
Bit Name							CS9	CS8

Reading from these registers give the button ON/OFF status.

Bit	Name	Description
x	CSx	This bit gives the button ON/OFF status 0 Button OFF
		1 Button ON

Acronyms

Acronym	Description
AC	alternating current
AI	analog input
AIO	analog input/output
AIDO	analog input/digital output
ARST	Auto Reset
DI	digital input
DO	digital output
DIO	digital input/output
P	power pins
C_F	finger capacitance
C_P	parasitic capacitance
CS	CapSense
FSS	flanking sensor suppression
GPO	general purpose output
I/O	input/output
LED	light emitting diode
LSB	least significant bit
MSB	most significant bit
PCB	printed circuit board
POR	power-on reset
POST	power on self test
QFN	quad flat no-lead
RF	radio frequency
SNR	signal to noise ratio

Document Conventions

Units of Measure

Units	Description
°C	degree Celsius
kΩ	kilohm
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
mil	one thousandth of an inch (1 mil = 0.0254 mm)
ms	millisecond
mV	millivolt
nA	nanoampere
nF	nanofarad
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volts

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, 01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.

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**	3698907	UDYG	07/31/2012	New datasheet
*A	3733388	UDYG	09/04/2012	Language edits. FMEA feature - required button resistance mentioned EZ-Click hyperlink fixed Move datasheet to final version
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*C	4888521	DIMA	08/18/2015	Updated to new template. Completing Sunset Review.
*D	5734095	AESATMP7	05/12/2017	Updated Cypress Logo and Copyright.

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