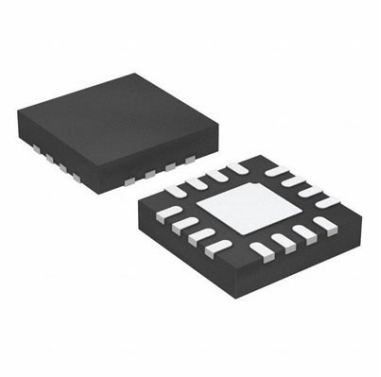
DS90UH948TNKDRQ1

LVDS Deserializer 3360Mbps 0.36V Automotive 64-Pin WQFN EP T/R



Images are for reference only

Inquiry

Manufacturer:	Texas Instruments, Inc
Package/Case:	WQFN64
Product Type:	Drivers
RoHS:	RoHS Compliant/Lead free
Lifecycle:	Active

General Description

The DS90UH948-Q1 is a FPD-Link III deserializer which, in conjunction with the DS90UH949A/949/947-Q1 serializers, converts 1-lane or 2-lane FPD-Link III streams into a FPD-Link (OpenLDI) interface. The deserializer is capable of operating over cost-effective 50-Ω single-ended coaxial or 100-Ω differential shielded twisted-pair (STP) cables. It recovers the data from one or two FPD-Link III serial streams and translates it into dual pixel FPD-Link (8 LVDS data lanes + clock) supporting video resolutions up to 2K (2048x1080) with 24-bit color depth. This provides a bridge between HDMI enabled sources such as GPUs to connect to existing LVDS displays or application processors.

The FPD-Link III interface supports video and audio data transmission and full duplex control, including I2C and SPI communication, over the same differential link. Consolidation of video data and control over two differential pairs decreases the interconnect size and weight and simplifies system design. EMI is minimized by the use of low voltage differential signaling, data scrambling, and randomization. In backward compatible mode, the device supports up to WXGA and 720p resolutions with 24-bit color depth over a single differential link.

The device automatically senses the FPD-Link III channels and supplies a clock alignment and de-skew functionality without the need for any special training patterns. This ensures skew phase tolerance from mismatches in interconnect wires such as PCB trace routing, cable pair-to-pair length differences, and connector imbalances.

Key Features

Qualified for automotive applications

AEC-Q100 qualified with the following results:

Device temperature grade 2: –40°C to +105°C ambient operating temperature

Supports pixel clock frequency up to 192 MHz for up to 2K (2048x1080) resolutions with 24-bit color depth

1-Lane or 2-lane FPD-Link III interface with de-skew capability

Single or dual OpenLDI (LVDS) transmitter

Single channel: up to 96-MHz pixel clock

Dual channel: up to 192-MHz pixel clock

Configurable 18-Bit RGB or 24-bit RGB

Integrated HDCP cipher engine with on-chip key storage

Supports HDCP repeater applications

Functional Safety-Capable

Documentation available to aid ISO 26262 system design

Four high-speed GPIOs (up to 2 Mbps each)

Adaptive receive equalization

Compensates for channel insertion loss of up to –15.5 dB at 1.48 GHz and -9 dB at 1.68 GHz

Provides automatic temperature and cable aging compensation

SPI control interfaces up to 3.3 Mbps

I2C (Controller/Target) With 1-Mbps fast-mode plus

Image enhancement (white balance and dithering)

Supports 7.1 multiple I2S (4 data) channels

Recommended For You

SN65LVDS3486D

Texas Instruments, Inc

SOP-16

SN65LVDS3487D

Texas Instruments, Inc

SOP16

DS90C032TM

Texas Instruments, Inc

SOP16

DS90C031BTM

Texas Instruments, Inc

SOP16

SN65LVDS31PW

Texas Instruments, Inc

TSSOP-16

SN65LVDS33D

Texas Instruments, Inc

SOP-16

SN65LVDS32D

Texas Instruments, Inc

SOP-16

SN65LVDS31D

Texas Instruments, Inc

SOP

SN65LVDS32PW

Texas Instruments, Inc

TSSOP16

DS90UB954TRGZTQ1

Texas Instruments, Inc

QFN48

DS90UB954TRGZRQ1

Texas Instruments, Inc

VQFN48

SN65DSI83TPAPRQ1

Texas Instruments, Inc

HTQFP-64

DS90UB947TRGCTQ1

Texas Instruments, Inc

VQFN-64

DS90LV011AQMF/NOPB

Texas Instruments, Inc

SOT23-5

DS90UB924TRHSTQ1

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WQFN-48