Qorivva MPC564xS Family
MCUs for instrument clusters

Overview

The Qorivva MPC564xS family is the next generation platform to follow the highly successful MPC560xS family designed to meet the needs of automotive instrument cluster market. The platform architecture includes on-chip display control units that directly drives the TFT displays. Further, there is an industry standard graphics accelerator available to help drive sophisticated graphics such as simulated instrument cluster needles or image warping for heads-up displays. In addition to large built-in memory, Quad SPI and DDR interfaces facilitate the possibility of accessing additional external memory. Finally, the Qorivva MPC564xS products offer code compatibility to customers already developing applications in the MPC560xS environment.

Applications

- Instrument cluster
- Central display

Enablement Ecosystem

The Qorivva MPC564xS family of MCUs is supported by similar tools as Freescale's Qorivva MPC5xxx products, offering a widespread, established network of tools and software vendors. It also features a high-performance Nexus 5001 debug interface.

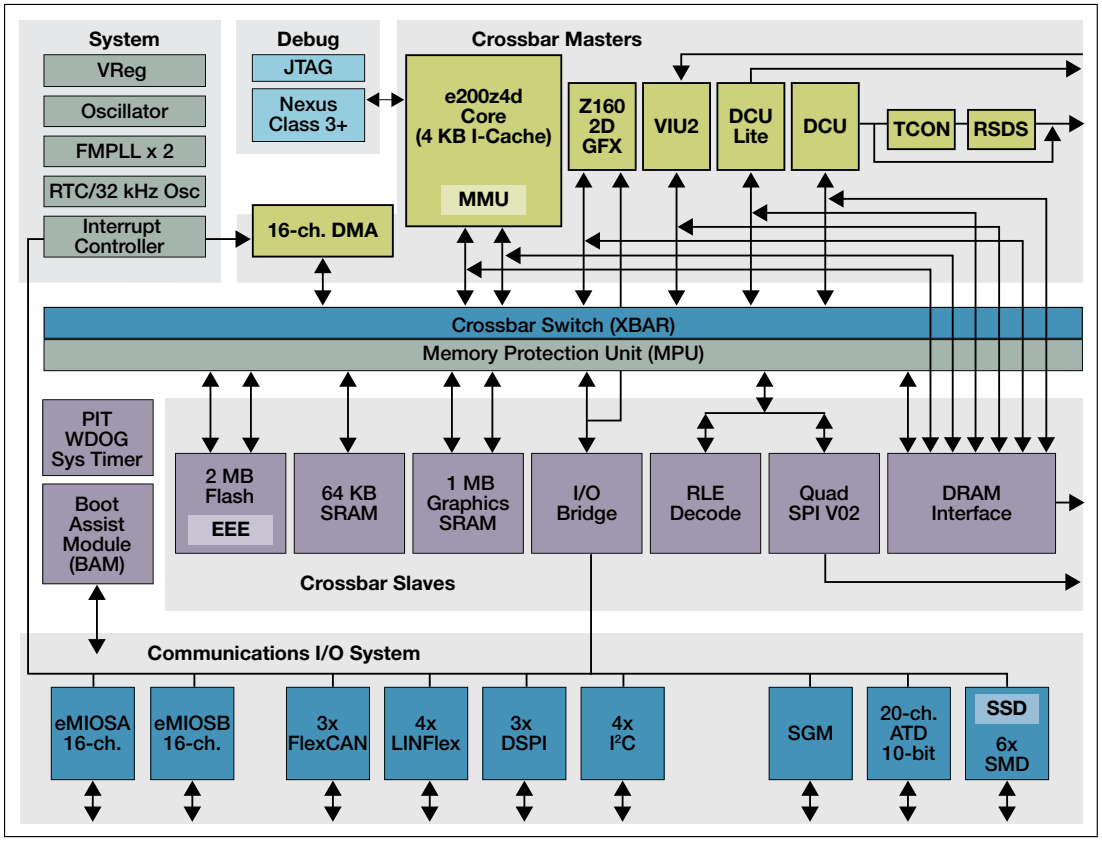
The following development support is now available:

- Automotive evaluation boards (EVBs) featuring CAN, LIN interfaces and more
- Compilers
- Debuggers
- JTAG and Nexus 5001 interfaces

The following software support is now available:

- OSEK solutions from multiple third parties
- CAN and LIN drivers

Qorivva MPC5645S 416-BGA



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Selector Guide

Product Number	Temp. Ranges	Features	Package	Speed
MPC5645S	-40°C to +105°C	e200z4d core, up to 125 MHz, 2 MB flash, 4 x 16 KB EEPROM emulation block (ECC), 64 KB RAM, 1 MB graphics RAM, 16 entry MPU, 16-ch. eDMA	416BGA, 208 LQFP, 176 LQFP	125 MHz

Development Tools

Part Number	Description	Pricing*
MPC5645SEVB	Kit includes development system and evaluation software	$299

*Manufacturer Suggested Resale Price

Documentation

Freescale Document Number	Title	Description
MPC564xSPB	MPC5645S Microcontroller Product Brief	Device family summary

Low Power Design

- Designed for dynamic power management of core and peripherals
- Software-controlled clock gating of peripherals
- Multiple power domains to minimize leakage in low power modes

Key Features

- Dual-issue, 32-bit Power Architecture Book E compliant CPU core complex (e200z4d) Memory management unit and 4 KB instruction cache
  - Variable length encoding (VLE) instruction set enables significant code size reduction over conventional Book E-compliant code
- Up to 2 MB on-chip flash with flash controller
- Separate 4 x 16 KB flash block for EEPROM emulation
- Up to 64 KB on-chip SRAM with ECC
- Up to 1 MB on-chip graphics SRAM (no ECC)
- Two TFT displays up to WVGA resolution parallel data interface (PDI) for digital video input
- Sound generation and playback using PCM or DDS sources with 4-channel mixer and PWM or I^2S outputs
- Stepper motor drivers with stepper stall detect for up to six gauges

Learn More: For more information about Qorivva MPX564xS family solutions, please visit **freescale.com/Qorivva**.

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