SN65DSI84TPAPRQ1

LVDS Receiver 1000Mbps Automotive 64-Pin HTQFP EP T/R

Manufacturer:	Texas Instruments, Inc
Package/Case:	HTQFP-64
Product Type:	Drivers
RoHS:	RoHS Compliant/Lead free
Lifecycle:	Active

SN65DSI84TPAPRQ1 Image

Images are for reference only

Inquiry

General Description

The SN65DSI84-Q1 DSI-to-LVDS bridge features a single-channel MIPI D-PHY receiver front-end configuration with four lanes per channel operating at 1 Gbps per lane and a maximum input bandwidth of 4 Gbps. The bridge decodes MIPI DSI 18-bpp RGB666 and 24-bpp RGB888 packets and converts the formatted video data-stream to an LVDS output operating at pixel clocks operating from 25 MHz to 154 MHz, offering a dual-link LVDS or single-link LVDS with four data lanes per link.

The SN65DSI84-Q1 device is well suited for WUXGA (1920 × 1080) at 60 frames per second (fps) with up to 24 bits-per-pixel (bpp). Partial line buffering is implemented to accommodate the data stream mismatch between the DSI and LVDS interfaces.

The SN65DSI84-Q1 device is implemented in a small outline 10 mm × 10 mm HTQFP package with a 0.5-mm pitch, and operates across a temperature range from –40°C to 105°C.

Key Features

Qualified for Automotive Applications

AEC-Q100 Qualified With the Following Results:
Device Temperature Grade 2: –40°C to 105°C Ambient Operating Temperature

Device HBM ESD Classification Level 3A

Device CDM ESD Classification Level C6

Implements MIPI D-PHY Version 1.00.00 Physical Layer Front-End and Display Serial Interface (DSI) Version 1.02.00

Single-Channel DSI Receiver Configurable for One, Two, Three, or Four D-PHY Data Lanes Per Channel Operating up to 1 Gbps Per Lane

Supports 18-bpp and 24-bpp DSI Video Packets with RGB666 and RGB888 Formats

Suitable for 60-fps WUXGA 1920 × 1200 Resolution at 18-bpp and 24-bpp Color, and 60-fps 1366 × 768 Resolution at 18-bpp and 24-bpp

Output Configurable for Single-Link or Dual-Link LVDS

Supports Single-Channel DSI to Dual-Link LVDS Operating Mode

LVDS Output-Clock Range of 25 MHz to 154 MHz in Dual-Link or Single-Link Mode

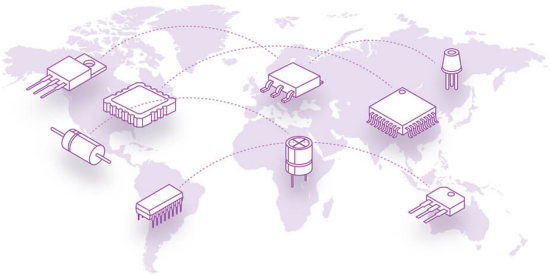
LVDS Pixel Clock May be Sourced from Free-Running Continuous D-PHY Clock or External Reference Clock (REFCLK)

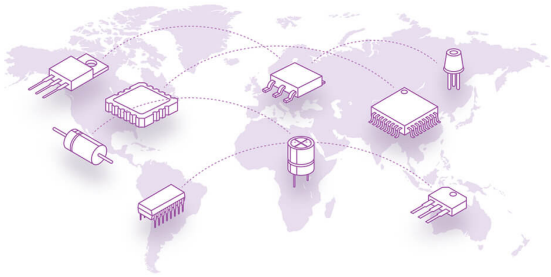
1.8 V Main V_{CC} Power Supply

Low Power Features Include SHUTDOWN Mode, Reduced LVDS Output Voltage Swing, Common Mode, and MIPI Ultra-Low Power State (ULPS) Support

LVDS Channel SWAP, LVDS PIN Order Reverse Feature for Ease of PCB Routing

Packaged in 64-pin 10 mm × 10 mm HTQFP (PAP) PowerPAD IC Package





AVAQ

AVAQ

Recommended For You

SN65LV1224BDBR

Texas Instruments, Inc

SSOP28

SN75173N

Texas Instruments, Inc

DIP

SN65LBC179D

Texas Instruments, Inc

SOP8

SN75176AD

Texas Instruments, Inc

SOP-8

SN65LVDS3486D

Texas Instruments, Inc

SOP-16

SN65HVD33MDREP

Texas Instruments, Inc

SOP-14

SN65LVDS3487D

Texas Instruments, Inc

SOP16

SN65LBC175AD

Texas Instruments, Inc

SOP-16

SN65LVDS31PW

Texas Instruments, Inc

TSSOP-16

SN75176AP

Texas Instruments, Inc

DIP8

SN65LVDS33D

Texas Instruments, Inc

SOP-16

SN65LVDS32D

Texas Instruments, Inc

SOP-16

SN65LVDS31D

Texas Instruments, Inc

SOP

SN75175D

Texas Instruments, Inc

SOP

SN75175N

Texas Instruments, Inc

DIP