


**Clock Generator 0.008MHz to 16.384MHz-IN 65.536MHz-OUT  
64-Pin TQFP Tray**

<b>Manufacturer:</b>	<a href="#">Microchip Technology, Inc</a>
<b>Package/Case:</b>	QFP
<b>Product Type:</b>	Clock & Timer ICs
<b>RoHS:</b>	RoHS Compliant/Lead free 
<b>Lifecycle:</b>	Active



Images are for reference only

[Inquiry](#)

### General Description

The ZL30100 T1/E1 System Synchronizer contains a digital phase-locked loop (DPLL), which provides timing and synchronization for multi-trunk T1 and E1 transmission equipment. The ZL30100 generates ST-BUS and other TDM clock and framing signals that are phase locked to one of two input references. It helps ensure system reliability by monitoring its references for accuracy and stability and by maintaining stable output clocks during reference switching operations and during short periods when a reference is unavailable. The ZL30100 is intended to be the central timing and synchronization resource for network equipment that complies with Telcordia, ETSI, ITU-T and ANSI network specifications. Simplified Block Diagram Typical Applications Synchronization and timing control for multi-trunk DS1/E1 systems such as DSLAMs, gateways and PBXs Clock and frame pulse source for ST-BUS, GCI and other time division multiplex (TDM) buses Line Card synchronization for PDH system

### Key Features

- Supports Telcordia GR-1244-CORE Stratum 4 and Stratum 4E
- Supports ITU-T G.823 and G.824 for 2048 kbps and 1544 kbps interfaces
- Supports ANSI T1.403 and ETSI ETS 300 011 for ISDN primary rate interfaces
- Simple hardware control interface
- Accepts two input references and synchronizes to any combination of 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz or 16.384 MHz inputs
- Provides a range of clock outputs: 1.544 MHz, 2.048 MHz, 16.384 MHz and either 4.096 MHz and 8.192 MHz or 32.768 MHz and 65.536 MHz
- Provides 5 styles of 8 kHz framing pulses
- Holdover frequency accuracy of  $1.5 \times 10^{-7}$
- Lock, Holdover and selectable Out of Range indication
- Selectable loop filter bandwidth of 1.8 Hz or 922 Hz
- Less than 0.5 nspp jitter on all output clocks
- External master clock source: clock oscillator or crystal

### Application

- Synchronization and timing control for multi-trunk DS1/E1 systems such as DSLAMs, gateways and PBXs
- Clock and frame pulse source for ST-BUS, GCI and other time division multiplex (TDM) buses
- Line Card synchronization for PDH system

## Recommended For You

---

### ZL30343GGG2

Microchip Technology, Inc  
BGA100

### ZL40213LDG1

Microchip Technology, Inc  
QFN

### ZL30143GGG2

Microchip Technology, Inc  
BGA

### ZL30105QDG1

Microchip Technology, Inc  
TQFP64

### ZL40200LDF1

Microchip Technology, Inc  
VQFN

### ZL30122GGG2

Microchip Technology, Inc  
BGA64

### ZL40200LDG1

Microchip Technology, Inc  
VQFN-16

### ZL40202LDG1

Microchip Technology, Inc  
new

### ZL30106QDG1

Microchip Technology, Inc  
QFP64

### ZL30266LDG1

Microchip Technology, Inc  
VQFN

### ZL40231LDG1

Microchip Technology, Inc  
VQFN-48

### ZL30157GGG2

Microchip Technology, Inc  
LBGA

### ZL30250LDG1

Microchip Technology, Inc  
QFN

### ZL40223LDG1

Microchip Technology, Inc  
VQFN-32

### ZL30117GGG2

Microchip Technology, Inc  
BGA