Application note

Driving a BLDC motor with the L99DZ200G

Introduction

The L99DZ200G is a system IC that provides electronic control modules with advanced power management, power capabilities, including various standby modes, as well as LIN and HS CAN physical communication levels, integrated power outputs and H-bridge gate drivers.

This application note is intended to provide a guide to users on how to drive a BLDC motor with the dual H-bridge gate drivers of the L99DZ200G.

1 Getting started

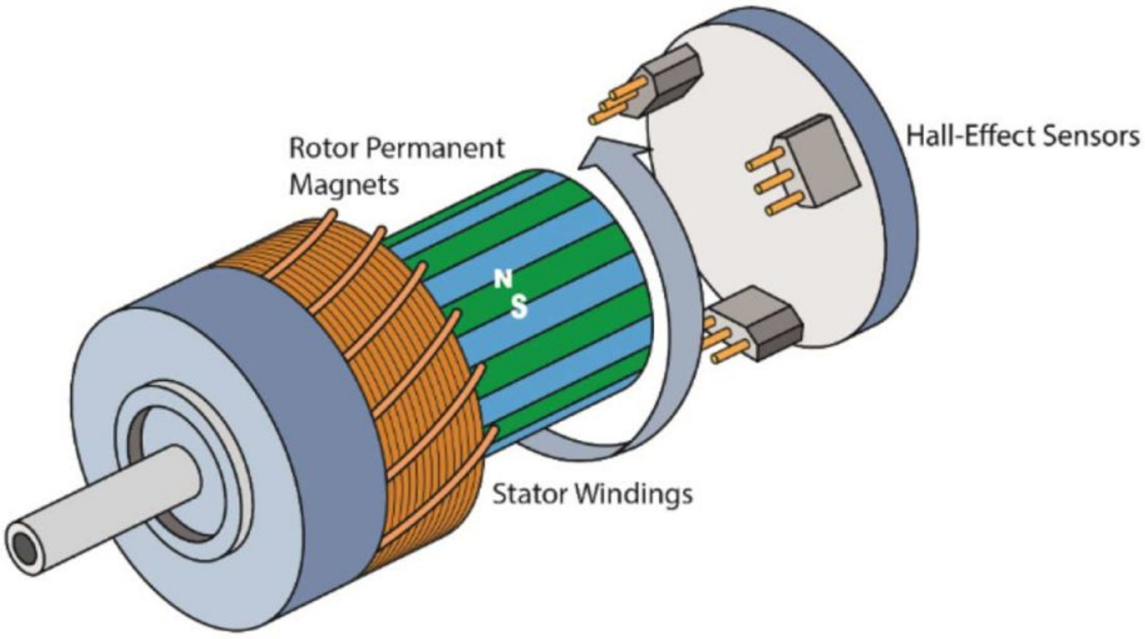
The L99DZ200G features two fully protected and programmable H-bridge drivers with dedicated drive inputs. Each of the two H-bridges (A and B) can operate in dual mode, for example as two independent half bridges. This means that the L99DZ200G is able to control four independent half bridges.

In this application note, three out of four of the two H-bridges configured in dual mode are used to drive a three-phases. BLDC motor, in six step mode that uses hall sensors as feedback of the rotor position.

2 BLDC motor

BLDC motors consist of a three-phase coil wound on a cylindrically magnetic core (the stator) and a rotor/shaft assembly which is normally held in position by bearings mounted at either end of the stator. The rotor is a smaller cylinder which is fixed to the shaft, concentric with the stator, and carries several permanent magnets mounted around its perimeter as shown in the figure below.

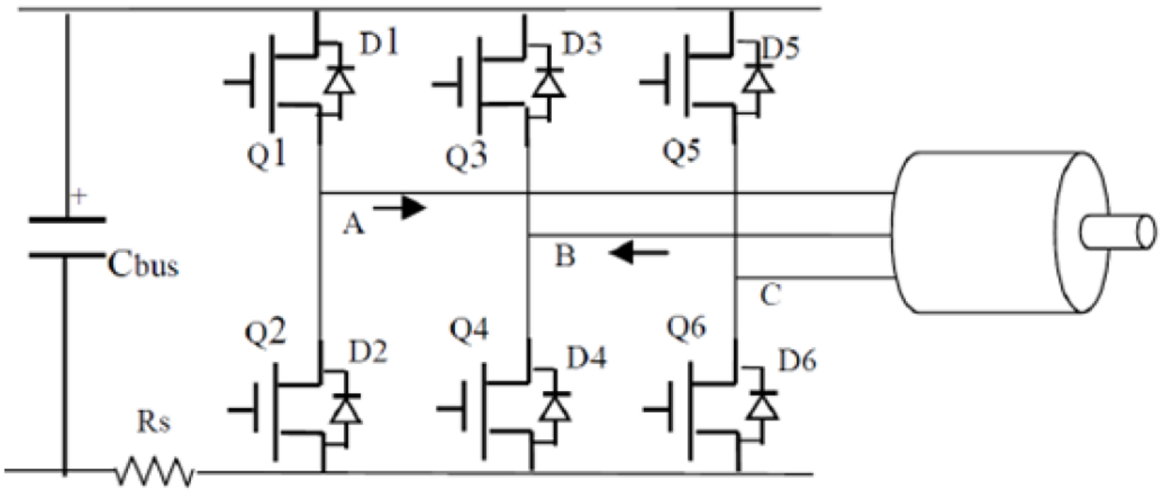
Figure 1. BLDC motor



The following figure shows the most common circuit topology for driving a three-phase brushless motor with a controlled full-bridge circuit with the PWM technique.

The equivalent circuit diagram with the three legs (one for each phase) consisting of two Power MOSFET devices for each leg.

Figure 2. Three-phase actuation circuit



The gates of the three legs HS-MOSFETS are driven by PWMH1A, PWMH2A and PWMH1B.

If you now assemble our BLDC motor and mechanically spin the rotor and you observe the voltage in A versus B on an oscilloscope you will observe a sinusoidal voltage. This is the Back Electro Motive Force (BEMF) of the motor.

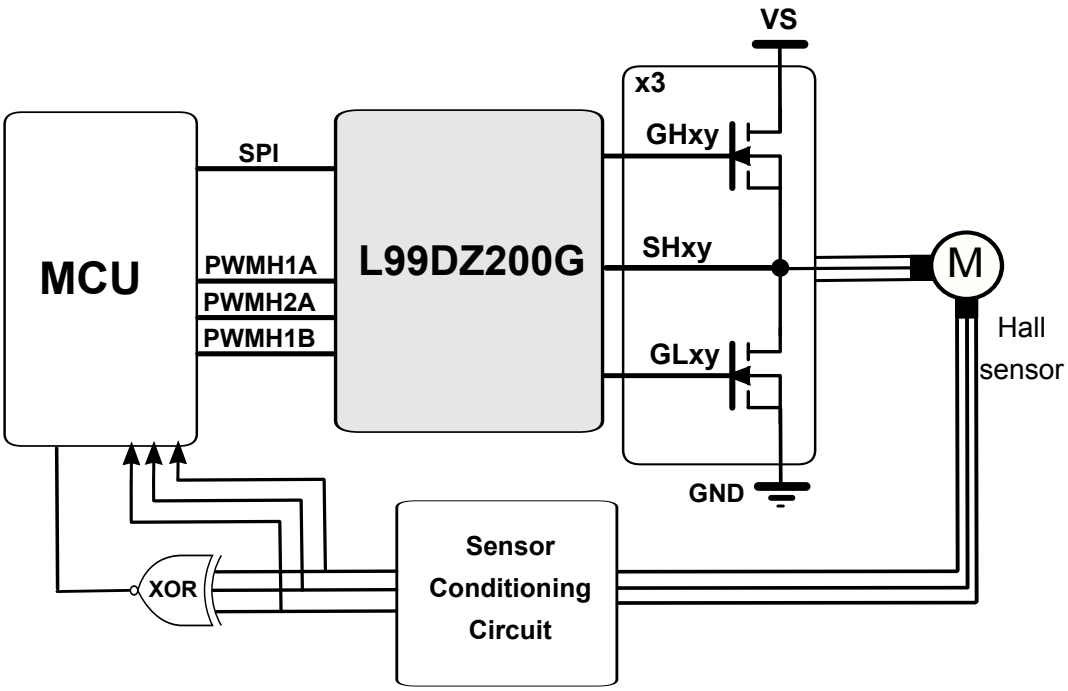
3 Application block diagram

In the application scenario illustrated below, the L99DZ200G is driven by a 32-bit MCU that can access its control registers via SPI and it can provide the three driving signals (PWMHsxy) for the three controlled external H-bridges. Although BEMF is available in every floating phase due to the six-phase drive mode, rotor position feedback is provided by the built-in engine room sensors, which provide the step commutation commands to the MCU.

Pitch switching events are triggered by the XOR output, which processes the signals from the hall sensors built into the motor (M). By reading the three hall sensor it is possible to drive the motor correctly.

The following figure depicts the application block diagram.

Figure 3. Application block diagram



4 L99DZ200G H-bridge drivers in dual mode

By setting the dual mode bit DMy (Config Reg) = 1, both the H-bridges of the H-bridge y (y=A, B) can be controlled independently through the dedicated input PWMHxy and dedicated control bits SDxy and SDSxy (Control Reg 10) according to the following figure:

Figure 4. H-bridge y (y = A, B) control truth table in dual mode (DMy = 1) for the leg x (x = 1, 2)

	Control pin	Control bits					Failure bits					Output pin		Comment
Nb	PWMHxy	HENy	DMy	DIRHy	SDxy	SDSxy	CP_LOW	VS_OV	VS_UV	DS	TSD1	GHxy	GLxy	
1	0	1	1	x	0	0	0	0	0	0	0	L	H	Active freewheeling LS
2	1	1	1	x	0	0	0	0	0	0	0	H	L	DRIVE HS
3	0	1	1	x	1	0	0	0	0	0	0	H	L	Active freewheeling HS
4	1	1	1	x	1	0	0	0	0	0	0	L	H	DRIVE LS
5	0	1	1	x	0	1	0	0	0	0	0	L	L	Passive freewheeling
6	1	1	1	x	0	1	0	0	0	0	0	H	L	DRIVE HS
7	0	1	1	x	1	1	0	0	0	0	0	L	L	Passive freewheeling
8	1	1	1	x	1	1	0	0	0	0	0	L	H	DRIVE LS

Operating the BLDC motor in six-phase mode means that during each phase there is a phase driven in PWM mode through the high-side MOSFETs with freewheel active on the corresponding low-side MOSFETs, one phase grounded and one left out. This driving signals scheme is obtained by driving each half bridge with the PWMHxy signal and setting the corresponding values of the control SDxy and SDSxy as described in the row 2, 4 and 5 inside the Figure 4. H-bridge y (y = A, B) control truth table in dual mode (DMy = 1) for the leg x (x = 1, 2). The rows 1 and 2 switch the corresponding half bridge xy output between battery and ground, the row 4 binds the corresponding half bridge xy output to ground and finally the row 5 sets the corresponding half bridge xy output in high impedance. Before driving the outputs, the two H-bridges must be enabled via the dedicated control bits HENA and HENB (Control Reg1) and must be configured in dual mode through dedicated bits DMA and DMB (Config Reg). Be careful that the L99DZ200G outputs may be disabled due to a watchdog error or any other error affecting the outputs, so the watchdog must be periodically updated and any source of error removed along with the corresponding flags that must be cleared. Drain source monitoring, cross current protection time and slew rates can be programmed via SPI according to application requirements (Control Reg10 and Control Reg21). The initial configuration of the outputs must not energize the motor coils.

5 Signals and output

The following figures show the driving signals (PWMH1A, PWMH2A and PWMH1B) together with the waveforms at the motor terminals. Since all control bits SDxy and SDSxy are in the same control register (Control Reg10), only one SPI access per pitch changing event is required to generate the appropriate output drive signals. During SPI access to the control register, PWMH1A, PWMH2A and PWMH1B should also be changed according to the six step mode-driving pattern.

Figure 5. VBAT=12 V, 30 KHz PWM with 20% duty cycle

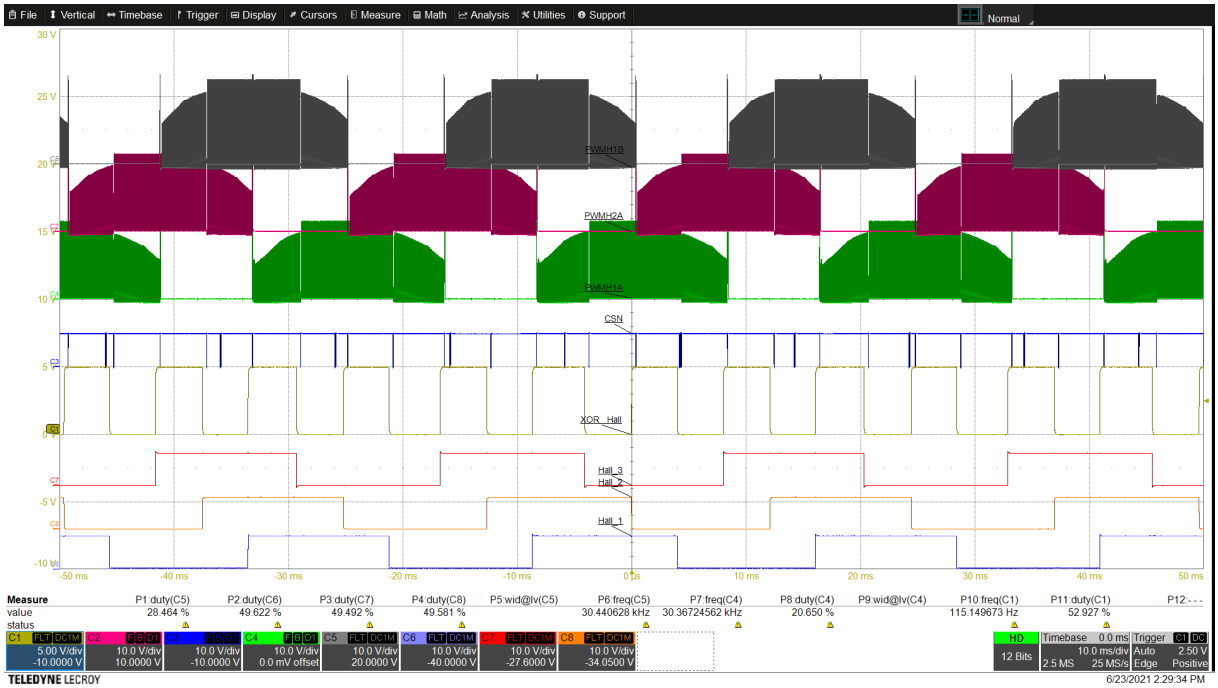
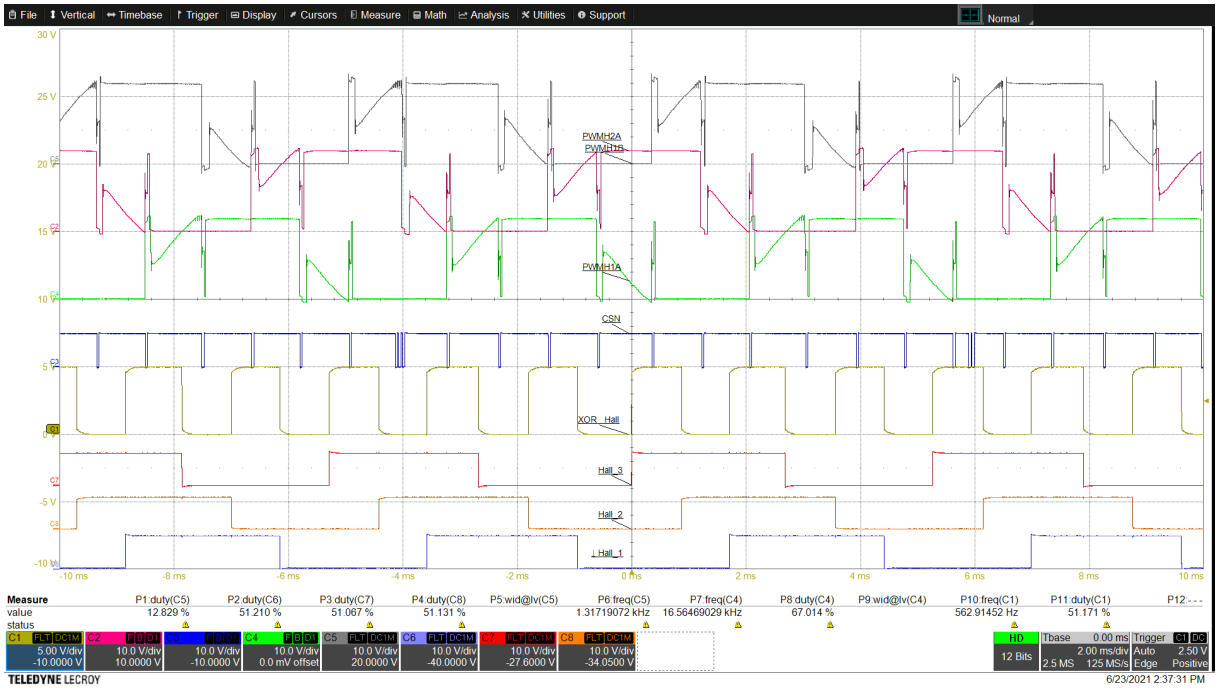


Figure 6. VBAT=12 V, 30 KHz PWM with 50% duty cycle

Figure 7. **VBAT=12 V, 30 KHz PWM with 100% duty cycle (10 ms/div.)**

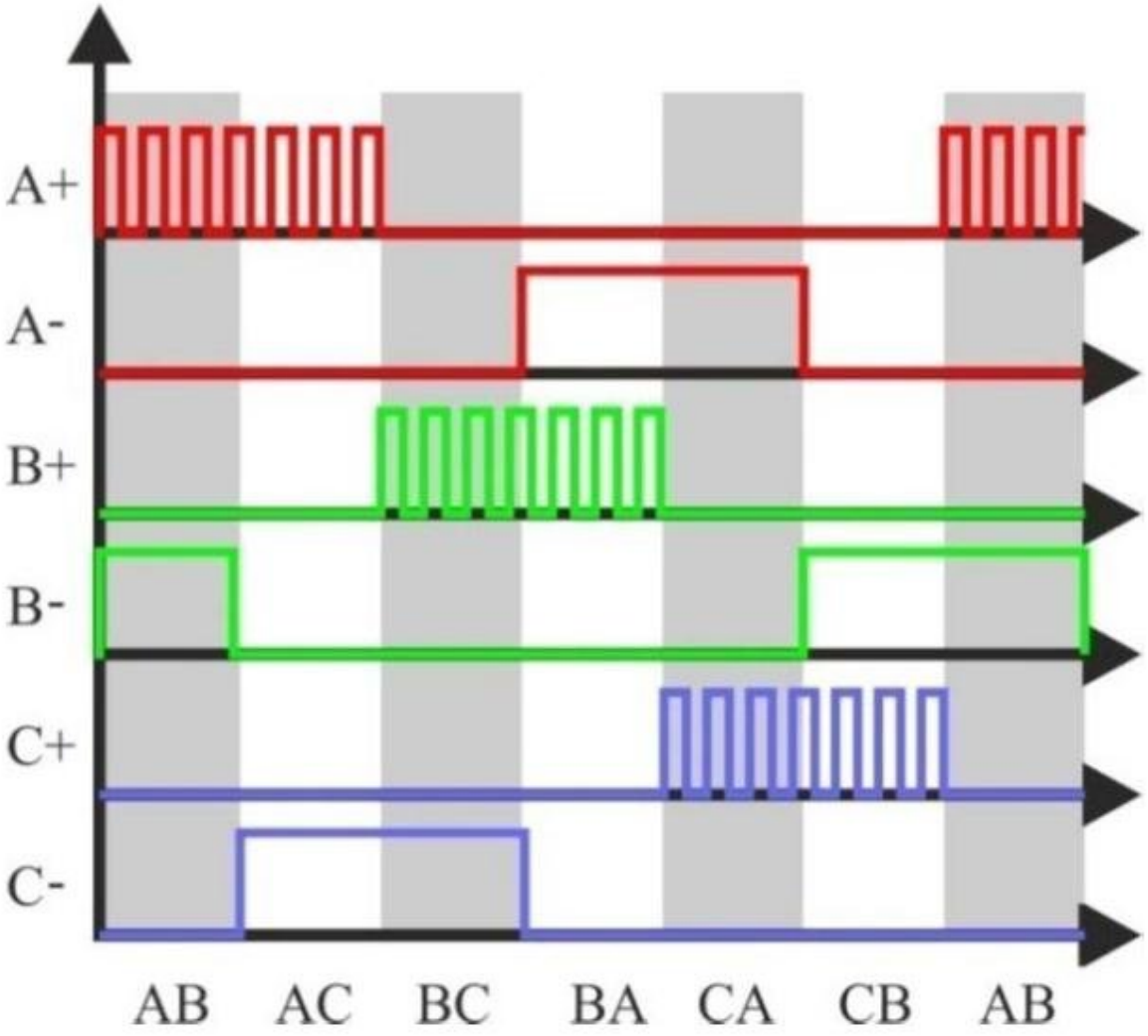
Figure 8. **VBAT=12 V, 30 KHz PWM with 100% duty cycle (2 ms/div.)**



6 Actuation

To actuate each step, it is needed to activate one high-side, one low-side and keep off the third leg. If we name A+ the first leg high-side, A- the first leg low-side while B and C refer respectively to the second and third leg, the correct actuation is:

Figure 9. 6 steps actuation



Actuation on BLDC motor is done by writing the CR10 according to the following table:

Table 1. Actuation

Steps	PWMH1B		PWMH2A		PWMH1A		Actuation	Leg Off	Decimal	HEX
	C		B		A					
	SD1B	SDS1B	SD2A	SDS2A	SD1A	SDS1A				
0	0	1	1	0	0	0	A+ B-	C Off	24	18
1	1	0	0	1	0	0	A+ C-	B Off	36	24
2	1	0	0	0	0	1	B+ C-	A Off	33	21
3	0	1	0	0	1	0	B+ A-	C Off	18	12
4	0	0	0	1	1	0	C+ A-	B Off	6	6
5	0	0	1	0	0	1	C+ B-	A Off	9	9

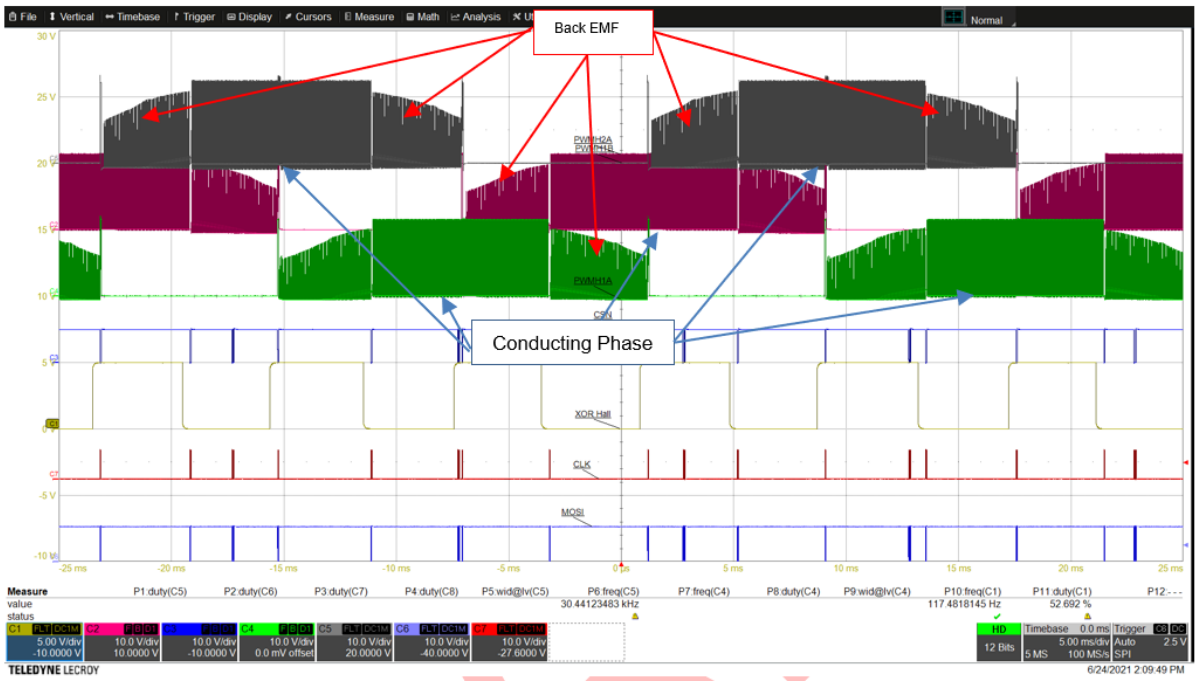
Table 2. H-bridge actuation

	Control pin	Control bits		Output pin		Comment
Nb	PWMHxy	SDxy	SDSxy	GHxy	GLxy	
1	0	0	0	L	H	Active freewheeling LS
2	1	0	0	H	L	DRIVE HS
3	0	1	0	H	L	Active freewheeling HS
4	1	1	0	L	H	DRIVE LS
5	0	0	1	L	L	Passive freewheeling
6	1	0	1	H	L	DRIVE HS
7	0	1	1	L	L	Passive freewheeling
8	1	1	1	L	H	DRIVE LS

An important event occurs during the reset phase when switching off a device changes the direction of the motor winding current. In this case the current continues to flow in the same direction, recirculating through the free-wheeling diodes (see the row 3 in Table 2. H-bridge actuation).

During the rotation of the motor, the effect of the BEMF can be observed. For a given motor, the amplitude and the frequency of the BEMF are both directly proportional to the rotor speed.

Figure 10. **BEMF and conducting phase**

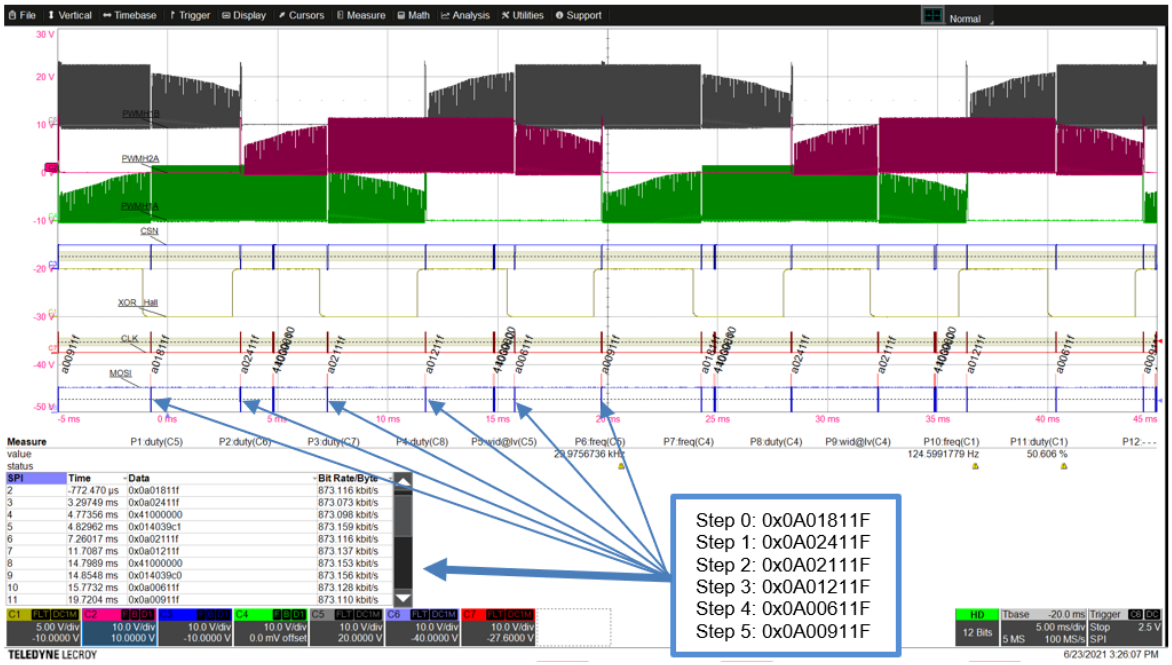


An interrupt is generated at each rising and falling edge of the XOR Hall sensors (Ch1- yellow signal in the below figures). Inside the interrupt routines, three hall sensor signals must be read, to select next steps.

Table 3. **6 step actuation**

Steps	Hall sensor			PWMH1B	PWMH2A	PWMH1A	Actuation
	c	b	a	C	B	A	
0	0	0	1	Off	1 on LS	PWMH1A on HS	A+ B-
1	0	0	0	1 on LS	Off	PWMH1A on HS	A+ C-
2	1	0	0	1 on LS	PWMH2A on HS	Off	B+ C-
3	1	1	0	Off	PWMH2A on HS	1 on LS	B+ A-
4	1	1	1	PWMH1B on HS	Off	1 on LS	C+ A-
5	0	1	1	PWMH1B on HS	1 on LS	Off	C+ B-

Figure 11. Step change Control Register 10 values and PWMHxy signals



In the previous SPI scan table, it is possible to observe the implementation of the six steps, between the watchdog frames, which occur every 10 ms (it is possible to choose another watchdog time: 10 ms, 50 ms, 100 ms, 200 ms).

7 Conclusions

L99DZ200G is able to fully control a BLDC motor thanks to its two integrated H-bridge drivers with dual mode.

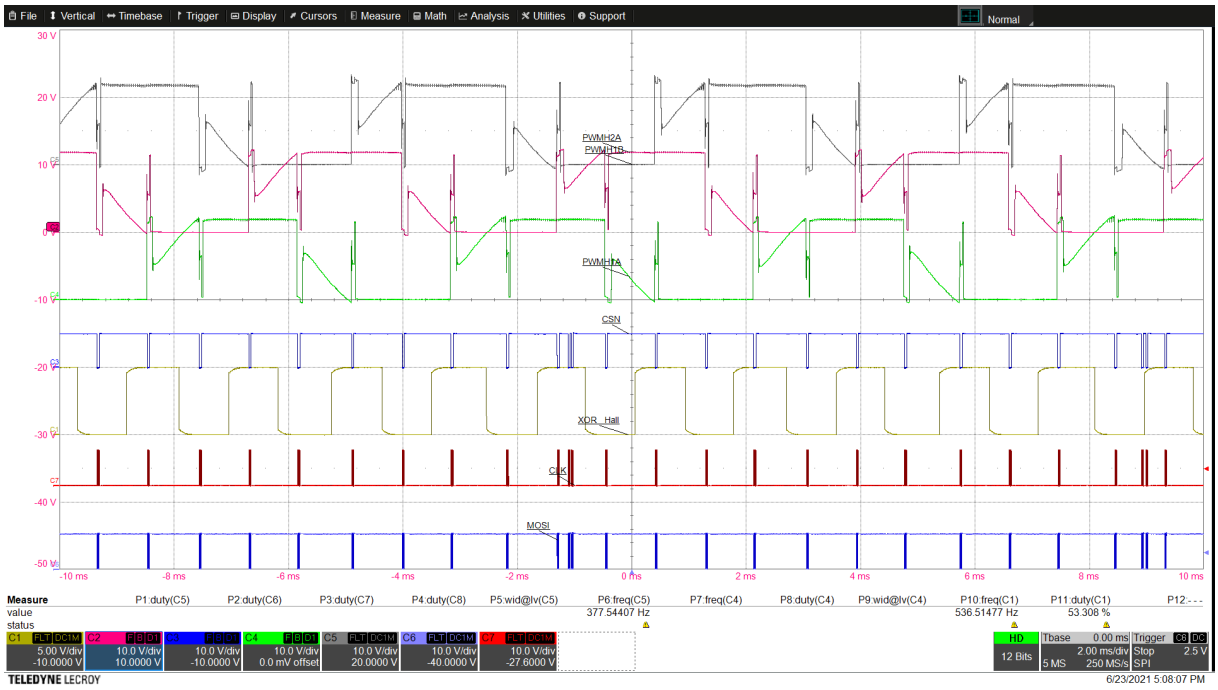
Since each switching step requires access to control register 10 L99DZ200G (address 0Ah), the switching speed of the step is limited by the SPI access speed required to correctly configure the outputs for the next step. However, this limitation only applies to very high frequency step switching BLDC motors.

In addition, SPI access to Control Register 1 (address 01h) is required to service the L99DZ00G watchdog periodically. With the following setup:

- SPI at 1Mbit/s
- watchdog at 10 ms (worst case)
- PWMHxy at 100% (max motor speed)

no failure has been observed.

Figure 12. VBAT=12 V, 30 KHz PWM with 100% duty cycle (2 ms/div.)



Revision history

Table 4. **Document revision history**

Date	Version	Changes
24-Nov-2021	1	Initial release.

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