Functional Safety Information

TLC6C5748-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TLC6C5748-Q1 (HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

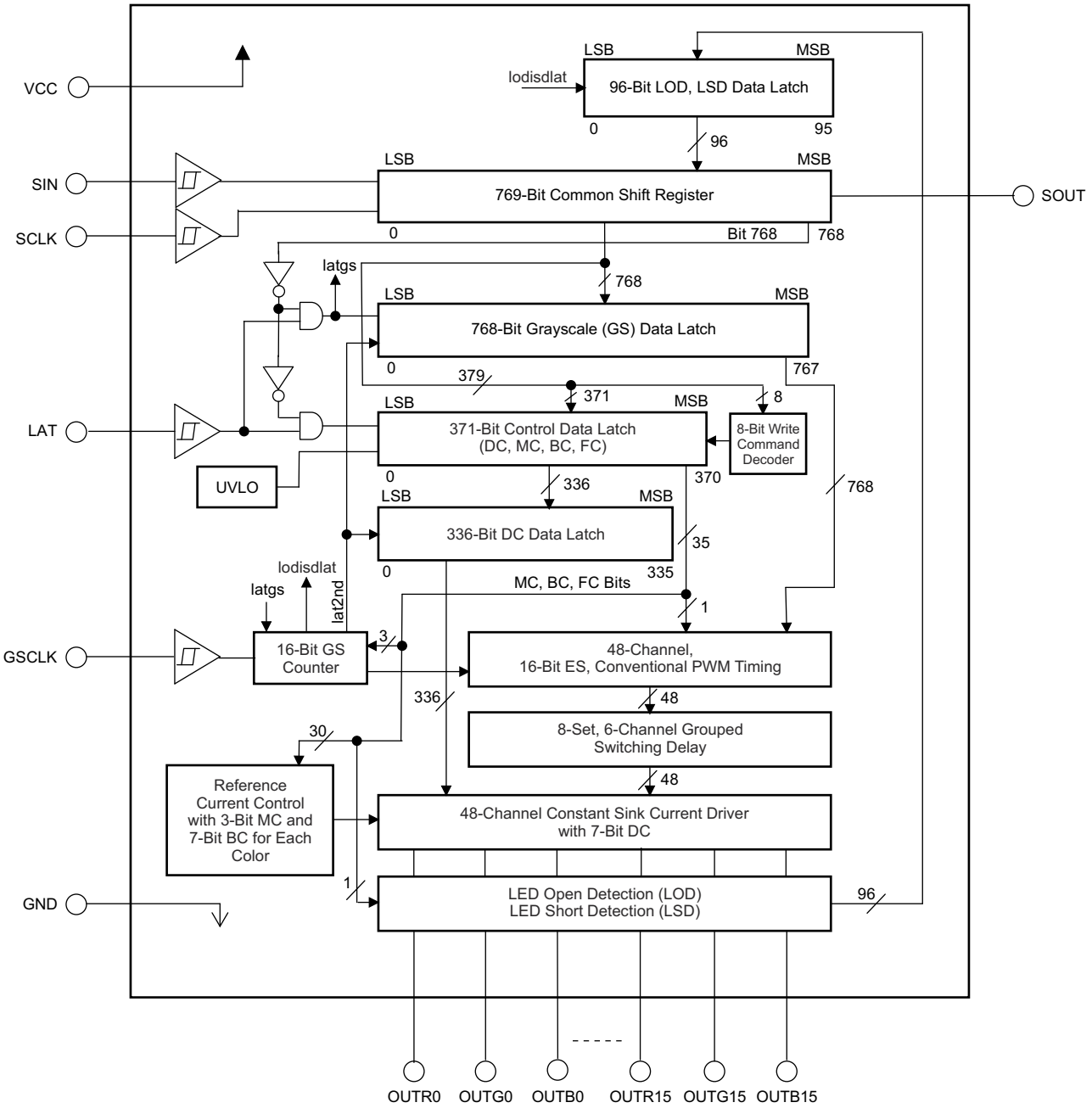

Figure 1-1. Functional Block Diagram

TLC6C5748-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TLC6C5748-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	44
Die FIT Rate	4
Package FIT Rate	40

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1000 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	60 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TLC6C5748-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Communication bus fail	1%
OUTn output out of specification, current or timing	57%
OUTn stuck off, communication bus fail	10%
OUTn stuck off, communication bus normal	5%
OUTn stuck on, communication bus fail	10%
OUTn stuck on, communication bus normal	5%
Fault fails to trip or false trip	12%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TLC6C5748-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VCC (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TLC6C5748-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TLC6C5748-Q1 data sheet.

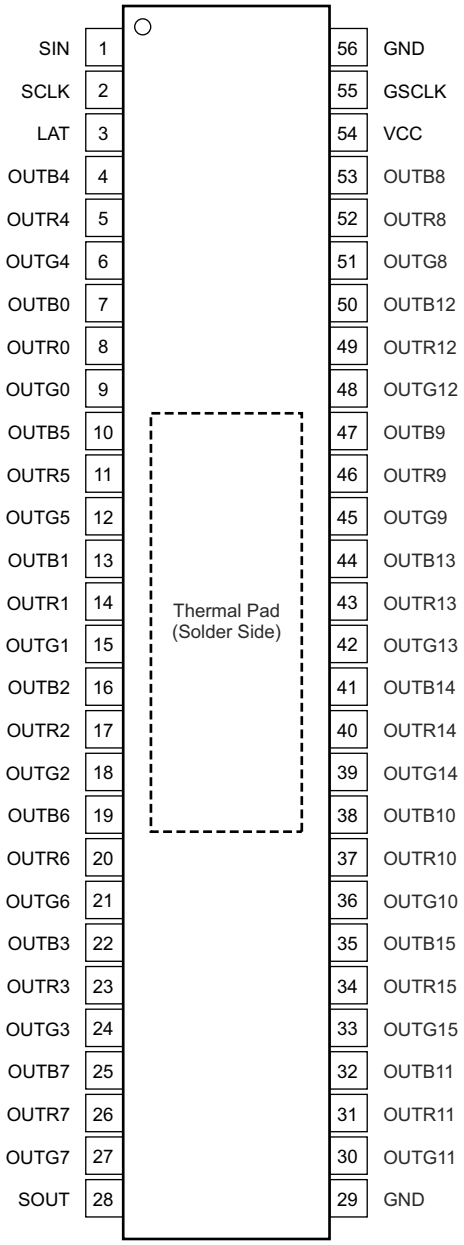

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Assume the device is running in the typical application. Please refer to the *Simplified Schematics* section in the TLC6C5748-Q1 data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SIN	1	The host controller can not control the device.	B
SCLK	2	The host controller can not control the device.	B
LAT	3	The host controller can not control the device.	B
OUTR0-7/ OUTG0-7/ OUTB0-7	4-27	Device report LOD	B
SOUT	28	The host controller can not read the device.	B
GND	29	No effect	D
OUTR8-15/ OUTG8-15/ OUTB8-15	30-53	Device report LOD	B
VCC	54	Device power off	B
GSCLK	55	Device can not output grayscale	B
GND	56	No effect	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SIN	1	The host controller can not control the device.	B
SCLK	2	The host controller can not control the device.	B
LAT	3	The host controller can not control the device.	B
OUTR0-7/ OUTG0-7/ OUTB0-7	4-27	Device report LOD	B
SOUT	28	The host controller can not read the device.	B
GND	29	Device not functional	B
OUTR8-15/ OUTG8-15/ OUTB8-15	30-53	Device report LOD	B
VCC	54	Device can not power up	B
GSCLK	55	Device can not output grayscale	B
GND	56	Device not functional	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
SIN	1	SCLK	The host controller can not control the device.	B
SCLK	2	LAT	The host controller can not control the device.	B
LAT	3	OUTB4	The host controller can not control the device.	B
OUTB4	4	OUTR4	Intended functionality	D
OUTR4	5	OUTG4	Intended functionality	D
OUTG4	6	OUTB0	Intended functionality	D
OUTB0	7	OUTR0	Intended functionality	D
OUTR0	8	OUTG0	Intended functionality	D
OUTG0	9	OUTB5	Intended functionality	D
OUTB5	10	OUTR5	Intended functionality	D
OUTR5	11	OUTG5	Intended functionality	D
OUTG5	12	OUTB1	Intended functionality	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUTB1	13	OUTR1	Intended functionality	D
OUTR1	14	OUTG1	Intended functionality	D
OUTG1	15	OUTB2	Intended functionality	D
OUTB2	16	OUTR2	Intended functionality	D
OUTR2	17	OUTG2	Intended functionality	D
OUTG2	18	OUTB6	Intended functionality	D
OUTB6	19	OUTR6	Intended functionality	D
OUTR6	20	OUTG6	Intended functionality	D
OUTG6	21	OUTB3	Intended functionality	D
OUTB3	22	OUTR3	Intended functionality	D
OUTR3	23	OUTG3	Intended functionality	D
OUTG3	24	OUTB7	Intended functionality	D
OUTB7	25	OUTR7	Intended functionality	D
OUTR7	26	OUTG7	Intended functionality	D
OUTG7	27	SOUT	The host controller can not control the device.	B
OUTG11	30	OUTR11	Intended functionality	D
OUTR11	31	OUTB11	Intended functionality	D
OUTB11	32	OUTG15	Intended functionality	D
OUTG15	33	OUTR15	Intended functionality	D
OUTR15	34	OUTB15	Intended functionality	D
OUTB15	35	OUTG10	Intended functionality	D
OUTG10	36	OUTR10	Intended functionality	D
OUTR10	37	OUTB10	Intended functionality	D
OUTB10	38	OUTG14	Intended functionality	D
OUTG14	39	OUTR14	Intended functionality	D
OUTR14	40	OUTB14	Intended functionality	D
OUTB14	41	OUTG13	Intended functionality	D
OUTG13	42	OUTR13	Intended functionality	D
OUTR13	43	OUTB13	Intended functionality	D
OUTB13	44	OUTG9	Intended functionality	D
OUTG9	45	OUTR9	Intended functionality	D
OUTR9	46	OUTB9	Intended functionality	D
OUTB9	47	OUTG12	Intended functionality	D
OUTG12	48	OUTR12	Intended functionality	D
OUTR12	49	OUTB12	Intended functionality	D
OUTB12	50	OUTG8	Intended functionality	D
OUTG8	51	OUTR8	Intended functionality	D
OUTR8	52	OUTB8	Intended functionality	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VCC

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SIN	1	The host controller can not control the device.	B
SCLK	2	The host controller can not control the device.	B
LAT	3	The host controller can not control the device.	B
OUTR0-7/ OUTG0-7/ OUTB0-7	4-27	Device report LSD	B
SOUT	28	The host controller can not control the device.	B
GND	29	Device can not power up	B
OUTR8-15/ OUTG8-15/ OUTB8-15	30-53	Device report LSD	B
VCC	54	No effect	D
GSCLK	55	Device can not output grayscale	B
GND	56	Device can not power up	B

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