AN5276
Application note

Antenna design for ST25R3916/16B, ST25R3917/17B, ST25R3918, and ST25R3920/20B devices

Introduction

One of the challenges in NFC technology is the design and matching of a proximity antenna according to a specific 13.56 MHz application. Very often, magnetic loop antennas are exposed to environmental conditions that degrade the system performance.

This application note is a design guide for magnetic loop antennas connected directly to the ST25R3916, ST25R3916B, ST25R3917, ST25R3917B, ST25R3918, ST25R3920, and ST25R3920B devices. Beyond the antenna design it describes the antenna parameter measurement and matching, as well as the design verification.

The examples in this document are based on the ST25R3916 device, but the techniques and tools can be used (when applicable) for other products of the same family.

The ST25R3916 is a high performance NFC front-end supporting NFC initiator, NFC target, NFC reader, and NFC card emulation modes.

The ST25R3916 includes an advanced analog front end (AFE) and a highly integrated data framing system for

- ISO 18092 (NFCIP-1) passive and active initiator, ISO 18092 (NFCIP-1) passive and active target
- NFC-A/B (ISO 14443A/B) reader including higher bitrates, NFC-F (FeliCa™) reader, and NFC-A and NFC-F card emulation. Special stream and transparent modes of the AFE and framing system can be used to implement other custom protocols such as MIFARE® Classic in reader or card emulation mode.

This document is intended to be used with the ST25R antenna matching tool software (STSW-ST25R004), which supports the calculation of the matching components and reduces the tuning iteration effort to a minimum. Along with the tool an open source simulator is provided for basic system validation via simulation.

The following documents are considered as reference:

- ST25R3916/16B, ST25R3917/17B, ST25R3918, and ST25R3920/20B datasheets, available on *www.st.com*
- AN4914, available on *www.st.com*
- ISO/IEC 14443 and ISO/IEC 10373-6:2011, from www.iso.org
- EMVCo, from www.emvco.com

Contents

List of tables

List of figures

1 List of acronyms and notational conventions

1.1 Acronyms

RFO1,2: Antenna driver output pins

RFI1,2: Receiver input pins

Tx: Transmit signal (from RFO to antenna)

Rx: Receive signal (from antenna to RFI)

$L_{EMC1,2}$: Inductor of the EMC filter

$C_{EMC1,2}$: Capacitor of the EMC filter

$C_{S1,2}$: Series capacitor of the matching network

C_P: Parallel capacitor of the matching network

R_Q: Parallel resistor used for the Q factor adjustment (calculated)

L_{ANT}: Antenna inductance (measured)

C_{ANT}: Parasitic antenna parallel capacitance (calculated)

R_{PANT}: Total antenna parallel resistance (calculated)

f_{work}: NFC operating frequency (13.56 MHz)

f_{res}: Antenna self-resonance frequency (measured)

R_{SDC}: Antenna series resistance (measured)

$R_{P@fres}$: Antenna parallel resistance at self-resonance (measured)

K: Skin effect correction factor (calculated)

$R_{P@work}$: Antenna parallel resistance at operating frequency (calculated)

R_{PDC}: Antenna parallel resistance converted from measured series resistance (calculated)

R_T: Parallel resistance for target Q factor (calculated)

Q: Antenna Q factor (calculated)

1.2 Representation of numbers

The following conventions and notations apply in this document unless otherwise stated:

- **Binary numbers** are represented by strings of 0 and 1 digits shown with the most significant bit (MSB) on the left, the least significant bit (LSB) on the right, and “0b” added at the beginning. Example: 0b11110101.
- **Hexadecimal numbers** are represented by using numbers 0 to 9 and characters A to F, and adding “0x” at the beginning. The Most Significant Byte (MSB) is shown on the left and the Least Significant Byte (LSB) on the right. Example: 0xF5.
- **Decimal numbers** are represented without any trailing character. Example: 245.

2 HW and SW requirements

To use the ST25R antenna matching tool, perform antenna measurements and verify the design, the following hardware and software resources are required:

- Network analyzer
- Oscilloscope (capable of pulse triggering)
- SMA cable
- ISO 10373-6 calibration coil 1
- ST25R3916-DISCO demonstration board
- Windows® OS
- ST25R antenna matching tool

3 Antenna interface stage

Figure 1 shows the minimum configuration for driving an antenna through a differential matching network, and *Figure 2* the circuit schematic.

From the ST25R3916 antenna driver output pins RFO1 and RFO2, the TX signal goes through the EMC filter into the matching network and to the antenna. The RX signal coming from the antenna is led through the capacitive voltage divider back into the ST25R3916 receiver input pins RFI1 and RFI2. The antenna interface stage can be set up as single ended or as differential topology, this document focuses on the latter configuration.

Figure 1. Antenna interface stage (differential matching network)

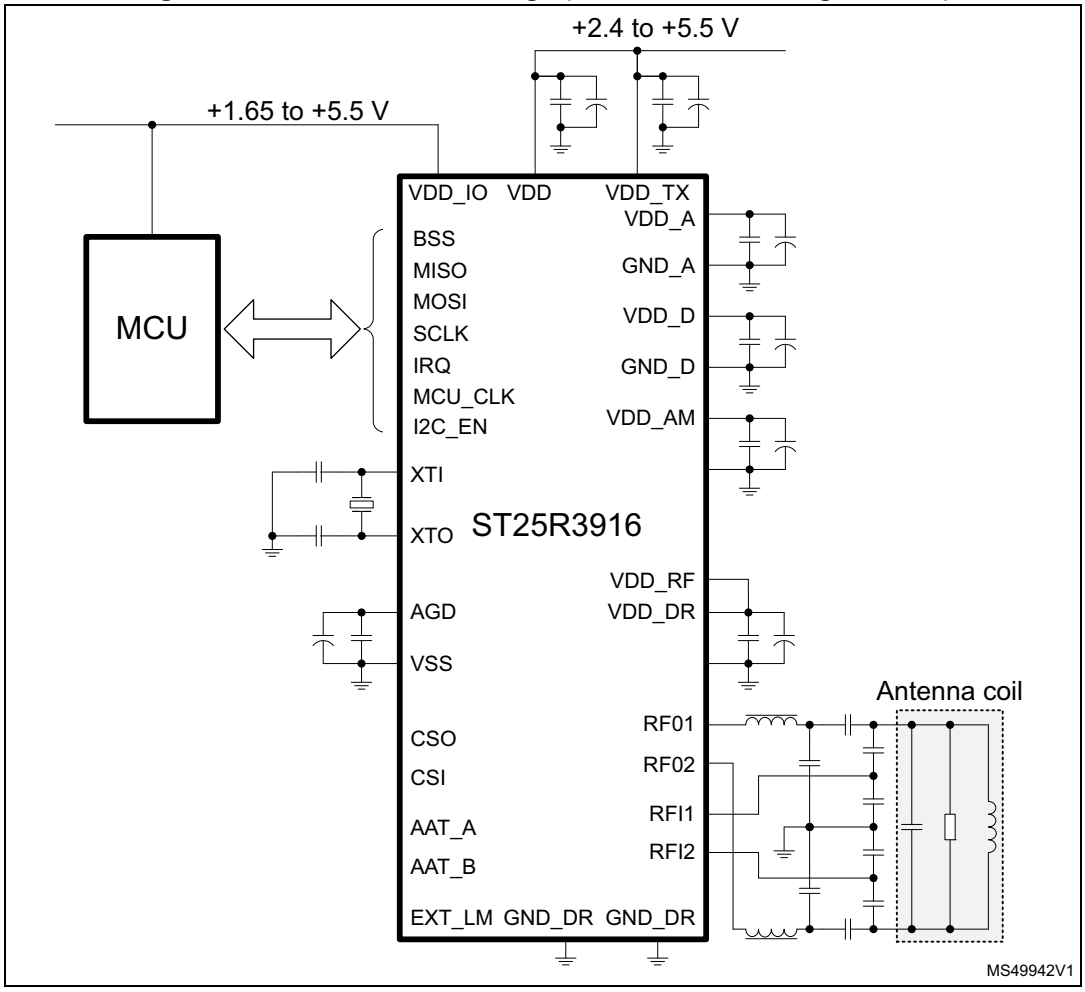
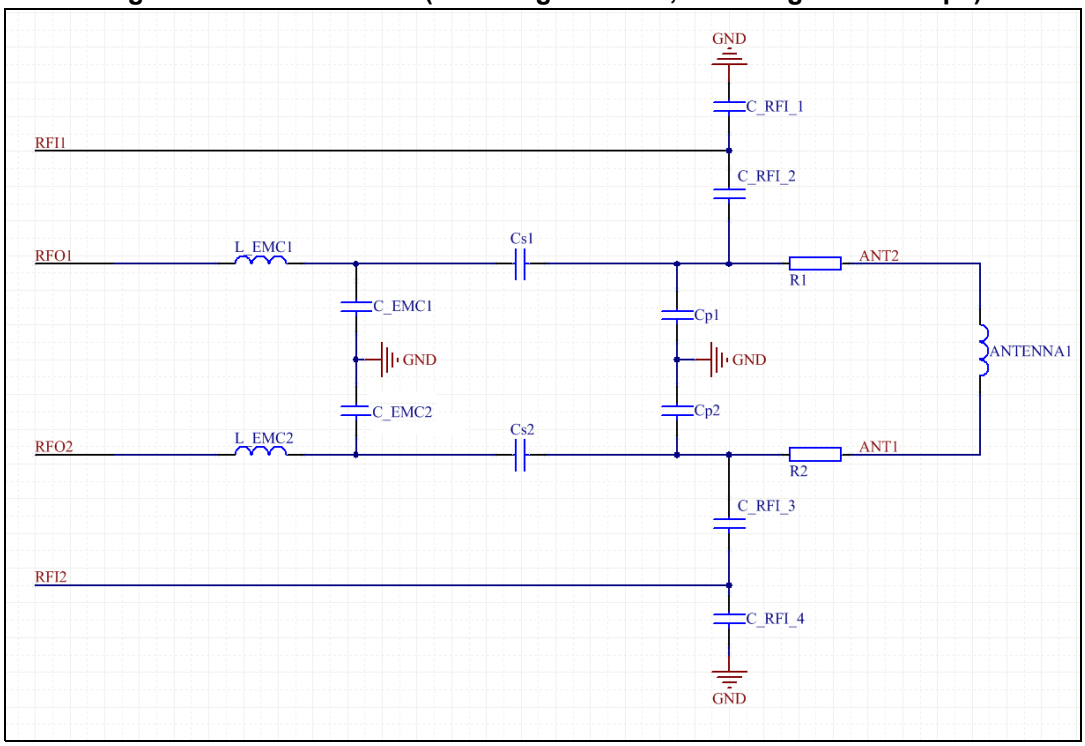


Figure 2. Antenna circuit (including EMI filter, matching and varicaps)



3.1 Card emulation mode

The card emulation mode places the ST25R3916 device in a passive communication mode. In card emulation mode the transmitter generates the load modulation signal by changing the resistance of the internal antenna driver connected to the antenna via RFO1 and RFO2. The same antenna and tuning circuitry as in reader mode can therefore be used.

Additionally, the transmitter can also drive an external MOSFET via the EXT_LM pin to generate the load modulation signal. This configuration can generate higher passive modulation levels than in “normal” mode, but requires additional components and a specific connection to the antenna.

3.1.1 Passive load modulation via internal driver

To prepare the device to passive load modulation through an internal driver, the passive target modulation register (address 29h, register space A) and the auxiliary modulation setting register have to be configured. The driver resistance is defined once for the modulated state (ptm_res) and once for the unmodulated state (pt_res) in the passive target modulation register. The largest modulation depth can be achieved by setting ptm_res<3:0> to Fh and pt_res<3:0> to 0h. It is also possible to use inverse polarity driver load modulation by using low impedance during non-modulated state and higher impedance for modulated state.

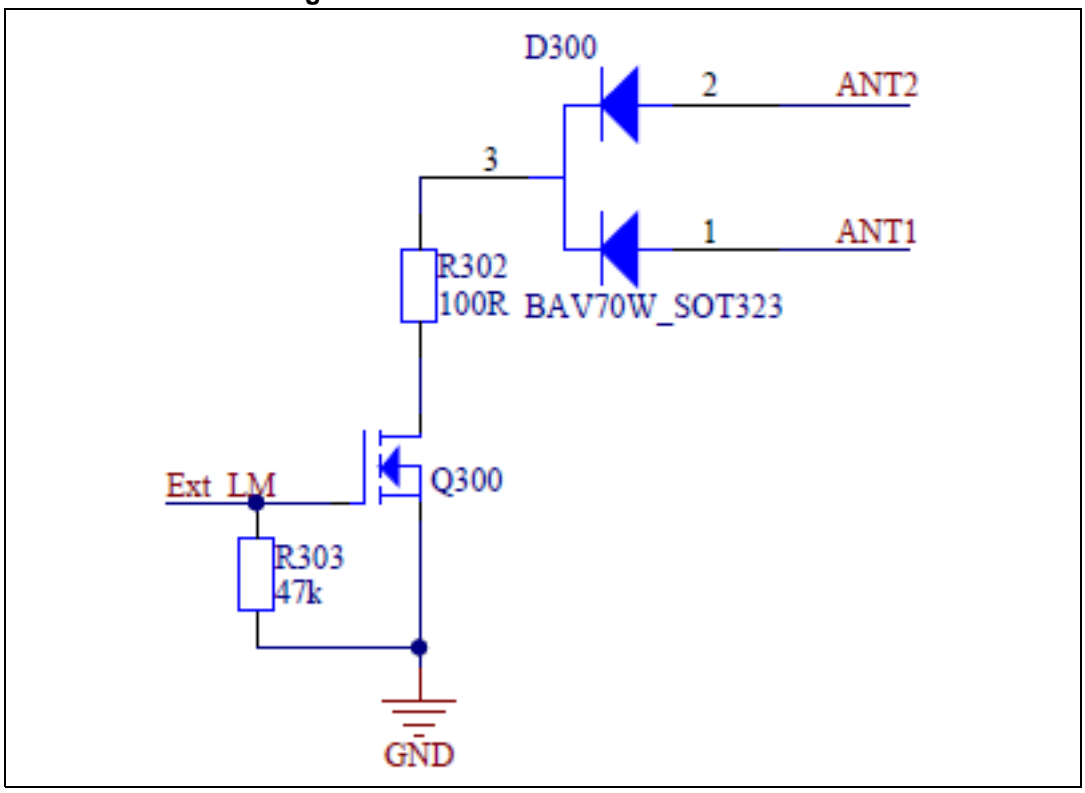
Furthermore, driver load modulation (lm_dri) bit needs to be enabled and external load modulation (lm_ext) disabled in the auxiliary modulation setting register at address 29h, register space B.

3.1.2 Passive load modulation via external transistor

External modulation through a MOSFET can be used for demanding applications where internal load modulation reaches its limits. The concept of using an external MOSFET is outlined in *Figure 3*, where the ext_lm pin is used to drive the gate of the external MOSFET.

The external modulation is enabled by enabling bit lm_ext and disabling lm_dri in the auxiliary modulation setting register. In this case the ext_lm pin is driven by digital representation of the load modulation signal (848 kHz subcarrier or 424/212 kHz modulation signal). The polarity of the modulation can be inversed by setting lm_ext_pol.

Figure 3. External load modulation circuit



3.2 Reader mode and output power

During the NFC/RFID reader design process several different requirements must be considered, a key one is the output power.

Different methods (among them capacitive or inductive wake-up) can be used to reduce the power consumption of the complete system. Besides using these power saving functions or reducing the power consumption by optimizing the polling cycle one very essential criterion is the power consumption during field on.

There are three steps to adjust the power consumption:

1. impedance matching
2. antenna driver output resistance (register 0x28)
3. chip internal regulator voltage

The impedance matching is the most important factor to determine the power consumption. When designing the matching circuitry and defining the target matching impedance, attention must be paid to *Figure 4*, showing that with higher target matching impedance less power is transferred forward to the antenna, and therefore the power consumption of the whole reader unit is reduced.

The last point to adjust the output power is the supply voltage of the driver stage. The V_{DD_RF} driver supply can be automatically set to V_{DD} minus the regulator dropout voltage. This is the optimal value for operation and noise rejection. It is also possible to manually overwrite the regulator setting and set V_{DD_TX} to a value specified in the datasheet.

The Smith chart in *Figure 4* shows the recommended matching impedance as a starting point in reader mode. By keeping the quality factor low as shown in *Figure 5*, the antenna system supports basic and higher bit rates for the different reader mode technologies. The matching and quality factor may have to be adapted to the user requirements in a second step.

Figure 4. Recommended matching impedance

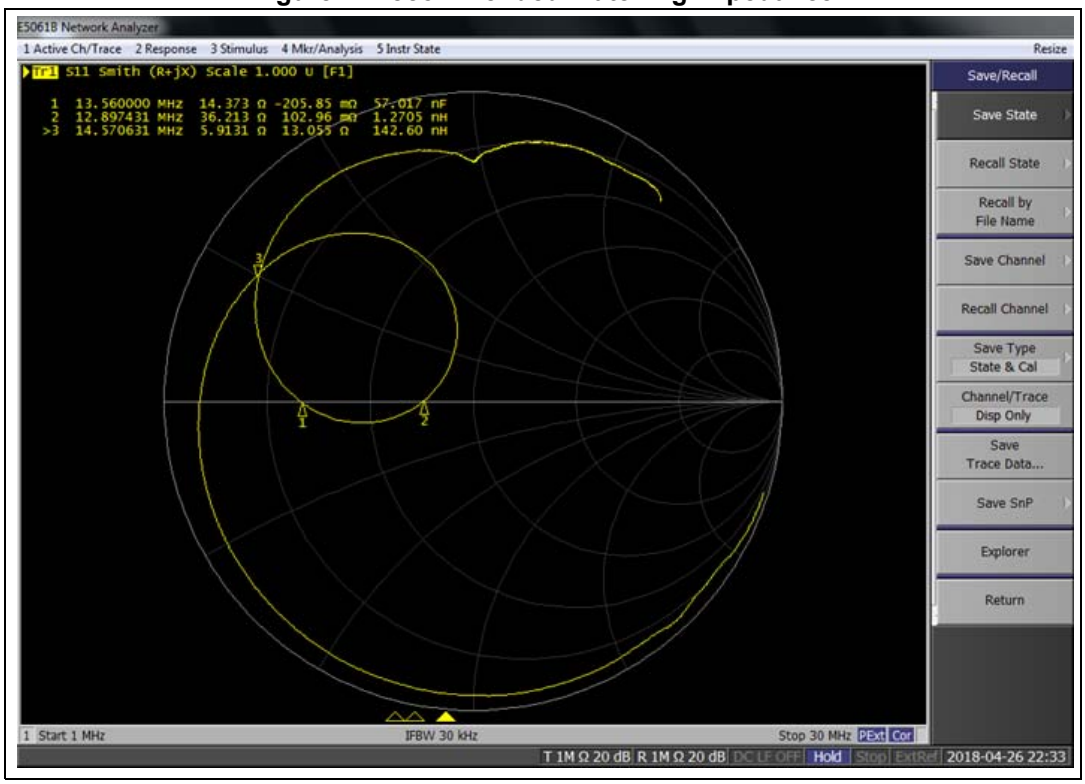
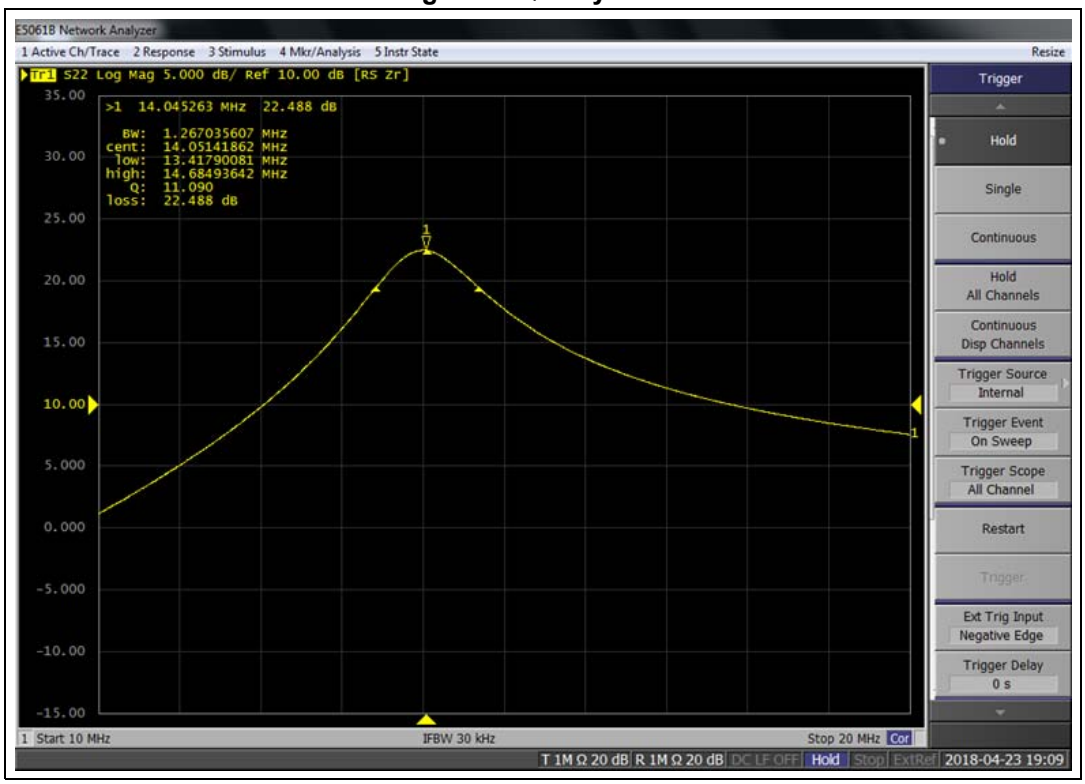


Figure 5. Quality factor



3.3 EMC filter

The EMC filter is implemented as a single stage low-pass filter consisting of a serial inductor and a parallel capacitor. The purpose of the EMC filter is to filter out higher harmonics caused by the rectangular output signal of the push-pull driver. The filter cutoff frequency should be between 8 and 17 MHz, the actual value depends on the application and the required behavior.

To optimize the EMC behavior of the reader board some considerations must be made:

- Filter coils:
  - Self-resonance frequency of the inductance: it can boost unwanted emissions in the investigated frequency range.
  - Equivalent serial resistance: influences the system Q factor of the reader, and can lower the conducted output power. EMC inductors with a higher ESR (>1 Ω) can only be used for mid and low power matchings. The ESR is put in series to the RFO output resistance. Therefore, higher ESR lower system Q factor and more power is lost in the EMC inductors.
  - Rated current of the chosen filter coils must be higher than the current in the matching network.
- Filter cut off frequency (filter resonance frequency):
  - If the filter cutoff frequency is too close to the carrier frequency (13.56 MHz), the system Q factor is strongly decreased. The reason is the combination of the

antenna and the filter Q factor. For this reason the EMC cutoff frequency must not be comprised between 13 and 14 MHz.

- Antenna design
  - The electrical length must be kept short to avoid additional self-resonances that boost unwanted emissions.

3.4 Matching network

The matching network in L topology follows the EMC filter and consists of one series and two parallel capacitors, in differential topology.

The purpose of the matching network is to match the antenna to a desired impedance value so that, depending on the application, either a maximum power transfer from the ST25R3916 to the antenna or a certain current consumption is achieved.

Figure 2 shows the antenna interface stage.

3.5 Capacitive voltage divider

As the voltage on the antenna can be high, a capacitive voltage divider is needed in the receive path at the antenna terminals to limit the signal strength going back to the RFI pins. This voltage divider is connected to the antenna and consists of two capacitors.

In *Figure 2* the capacitor pairs RFI_1/RFI_2 and RFI_3/RFI_4 form the capacitive voltage divider.

The voltage at the receive pins must not exceed 3 V_{pp}. In HF reader mode and NFC transmit mode recommended signal level is 2.8 V_{pp}.

3.6 Antenna

The antenna of the HF reader is a magnetic loop antenna, typically implemented as a printed coil. Flex-PCB, wire wound antennas or metal casing are other possible approaches.

Factors like size, number of tracks, track and gap width determine the electrical parameters of the antenna: inductance, series and parallel resistance, self-resonance frequency, and, most important of all, the Q factor.

The antenna must be designed with a Q factor higher than the target system Q factor. This is because the antenna Q factor can only be decreased by damping resistors afterwards, and not increased anymore.

4 Antenna parameters

Every antenna is composed of inductance, resistance and capacitance. These values and the self-resonance frequency of the antenna must be determined first to calculate the antenna equivalent circuit and its Q factor, and then determine the matching components.

4.1 Network analyzer preparation

In order to measure the antenna parameters a network or impedance analyzer shall be used and set up according to the procedure detailed below:

1. Set the measurement mode of the network analyzer to S11 reflection measurement
2. Use the Smith chart format (R + jX) to display the impedance curve
3. Set the start frequency at 1 MHz and the stop frequency at 300 MHz

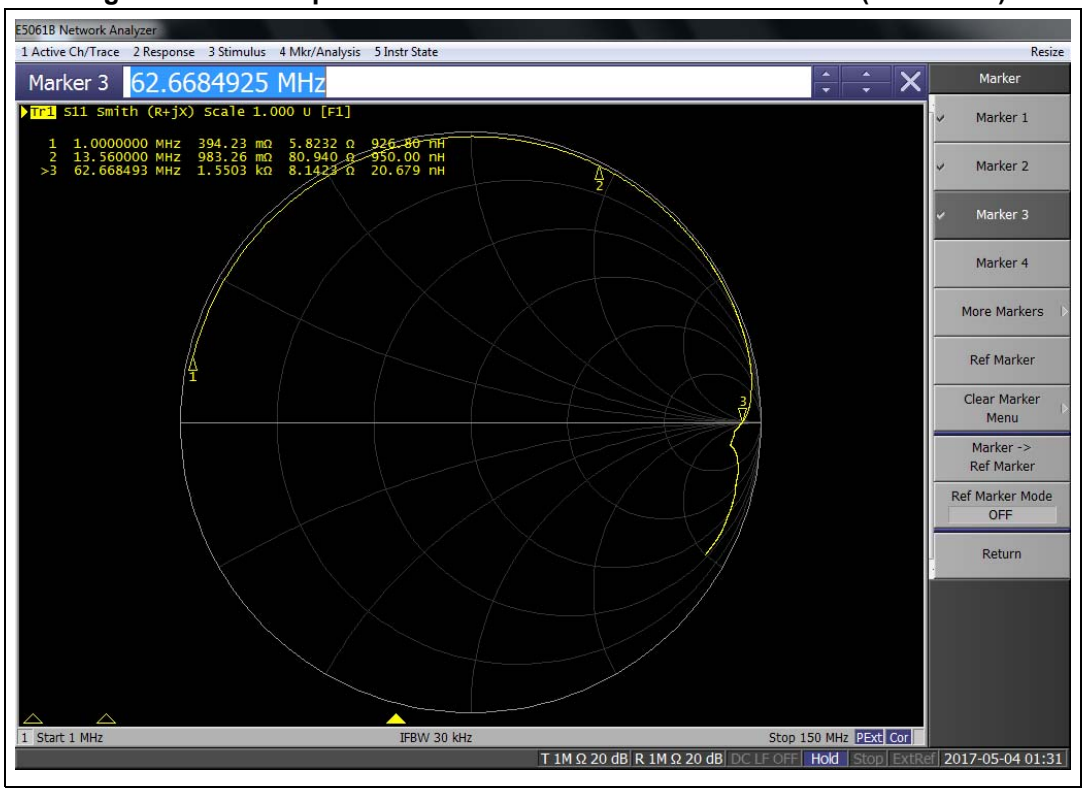
Note: Some of the antenna parameters are measured at 1 MHz, far off the self-resonance frequency of the antenna to minimize the skin effects measured at higher frequencies. The stop frequency must be higher than the first self-resonance frequency (usually between 50 and 250 MHz) of the reader antenna.

4. Set the network analyzer resolution (number of points) to the maximum to ensure accurate measurements
5. Connect a short SMA cable (<50 cm) to the RF port of the network analyzer and start the calibration using OPEN, SHORT and LOAD from a calibration kit or auto-calibration. If no calibration kit is available, a workaround with a 50 Ω resistance as load, as well as an open and short connection on the cable can be used. With the calibration the SMA cable length is accounted for.
6. To connect the SMA cable to the antenna to be measured, a probe connection from pins (one pin soldered to the signal connection of an SMA connector, the other one soldered to one of its ground connections) must be made.
7. The added pins can be taken into account for calibration with the auto port extension function of the VNA.

4.2 Parameter measurement

1. Connect the cable of the network analyzer at the antenna ends. The antenna has to be disconnected from the reader / matching network and the reader has not to be powered. Connecting a powered reader to a VNA can cause damage to the VNA.
2. The impedance curve from 1 to 300 MHz is displayed in the Smith chart (see*Figure 6*)
3. Set a marker to 1 MHz and read the series inductance and the DC series resistance values (in *Figure 6* they are displayed in the upper part of the network analyzer screen):
   - L_{ANT} = 926 nH
   - R_{SDC} = 394 mΩ
4. Set another marker to the real axis of the Smith chart, where the inductive and the capacitive part of the impedance cancel each other. At this point, the parallel resistance and the self-resonance frequency of the antenna are measured:
   - $R_{P@fres}$ = 1.55 kΩ
   - f_{res} = 62.67 MHz

Figure 6. Antenna parameter measurement at 1 MHz and SRF (62.67 MHz)



The antenna parameters have now been measured, and the equivalent circuit can be determined, as described in *Section 4.3*.

4.3 Antenna equivalent circuit

Using the antenna inductance measured at 1 MHz, the parasitic capacitance at self-resonance-frequency can be calculated as follows:

$$C_{ANT} = 1 / (\omega^2 * L) = 1 / [(2\pi * f_{res})^2 * L_{ANT}] = 1 / [(2\pi * 62.7\ MHz)^2 * 926\ nH] = 6.96\ pF$$

The measured value of the parallel resistance has to be converted from the self-resonance to the operating frequency (f_{work} = 13.56 MHz). The reason for this conversion is the correction for the frequency dependent change due to the skin effect. To convert the parallel resistance at the self-resonance frequency, a correction factor has to be calculated:

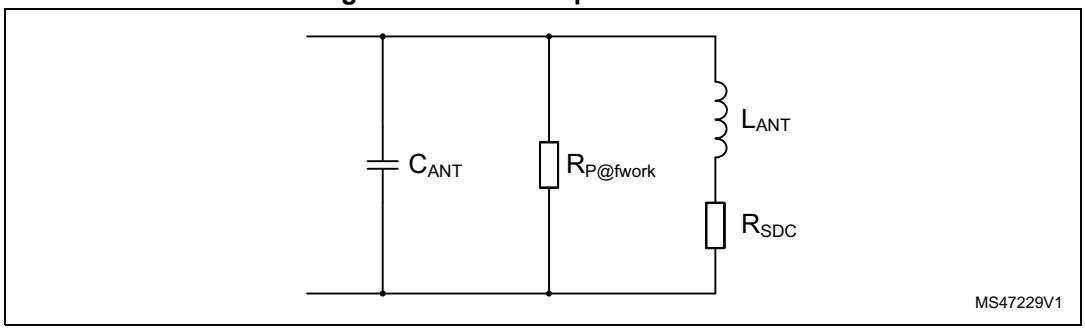
$$K = \sqrt{\frac{f_{res}}{f_{work}}} = \sqrt{\frac{62{,}7MHz}{13.56MHz}} = 2.15$$

The parallel resistance at the operating frequency is calculated as

$$R_{P@fwork} = K * R_{P@fres} = 2.15 * 1.55\ k\Omega = 3.33\ k\Omega$$

All antenna components are now known, so the equivalent circuit can be determined (see *Figure 7*).

Figure 7. Antenna equivalent circuit



The equivalent circuit can be simplified by recalculating the series resistance into a parallel resistance (see *Figure 8*) at the operating frequency, with the formula

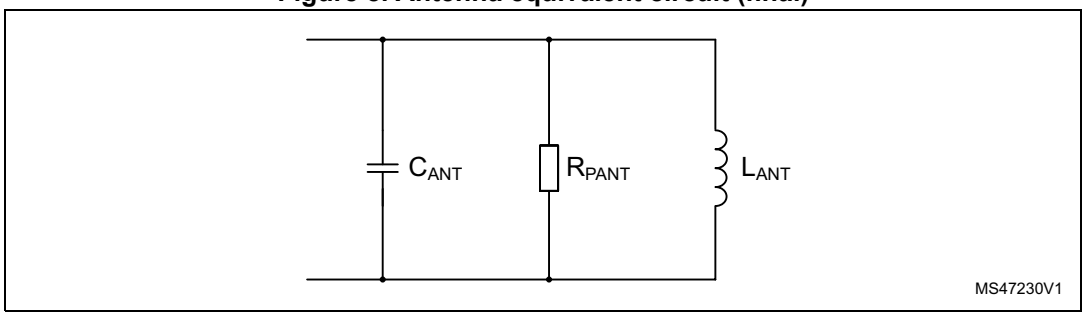
$$Q = \frac{\omega L_{ANT}}{R_{SDC}} \approx \frac{R_{PDC}}{\omega L_{ANT}} \Rightarrow R_{PDC} = \frac{(2 \cdot \pi \cdot f_{res} \cdot L_{ANT})^2}{R_{SDC}} = \frac{(2 \cdot \pi \cdot 13{,}56\text{MHz} \cdot 926\text{nH})^2}{394\text{m}\Omega} = 15.9\text{k}\Omega$$

The total resistance for the antenna equivalent circuit can be represented by a parallel resistance consisting only of the DC series resistance (recalculated into a parallel one), and the parallel resistance converted to the operating frequency.

Adding the two parallel resistances leads to the total parallel resistance

$$R_{PANT} = \frac{R_{PDC} \cdot R_{P@fwork}}{R_{PDC} + R_{P@fwork}} = \frac{15.9\Omega \cdot 3.33\text{k}\Omega}{15.9\text{k}\Omega + 3.33\text{k}\Omega} = 2.76\text{k}\Omega$$

Figure 8. Antenna equivalent circuit (final)



The values for the final and simplified antenna equivalent resonance circuit are:

- R_{PANT} = 2.76 kΩ
- C_{ANT} = 6.96 pF
- L_{ANT} = 926 nH

The maximum achievable Q factor for this antenna can now be calculated:

$$Q = R_{PANT} / (\omega * L_{ANT}) = 2.76\ \text{k}\Omega / (2\ \pi * 13.56\ \text{MHz} * 926\ \text{nH}) = 34.8$$

This Q factor is valid for the freely oscillating unconnected antenna.

The Q factor has a direct influence on the rise and fall times of the modulated signal.

Figure 9 and *Table 1* show the definition of rise and fall times for a Type-A signal modulated with 100% ASK and a data rate of 106 kbit/s (f_{work} / 128), while *Figure 10* is an example of their dependence on the Q factor.

Figure 9. Definition of timing parameters for Type-A with 106 kbit/s

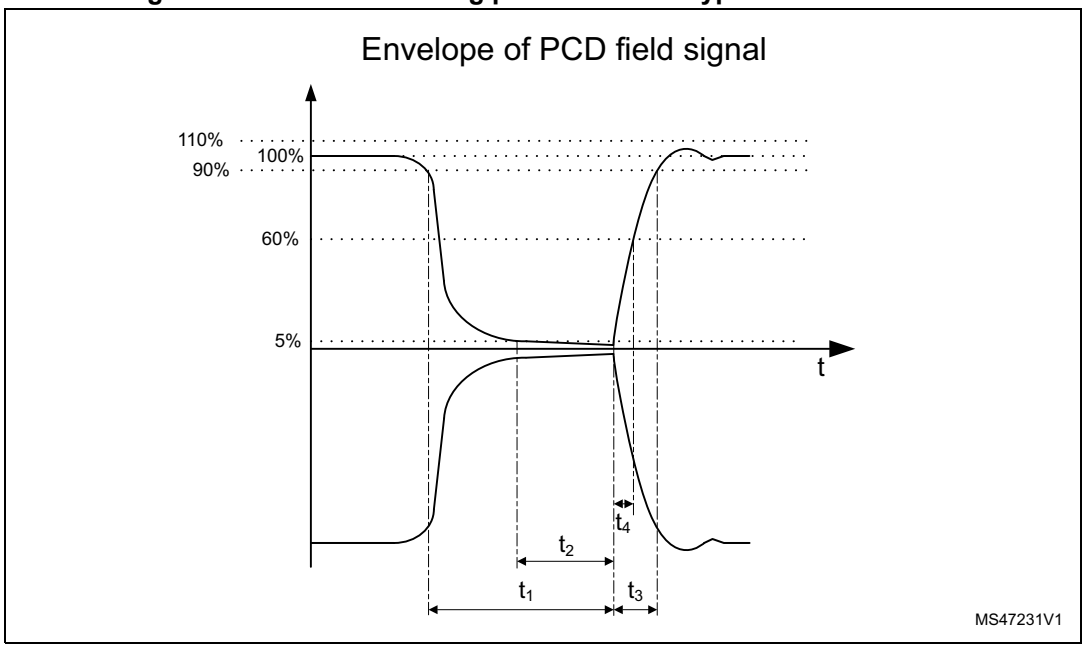
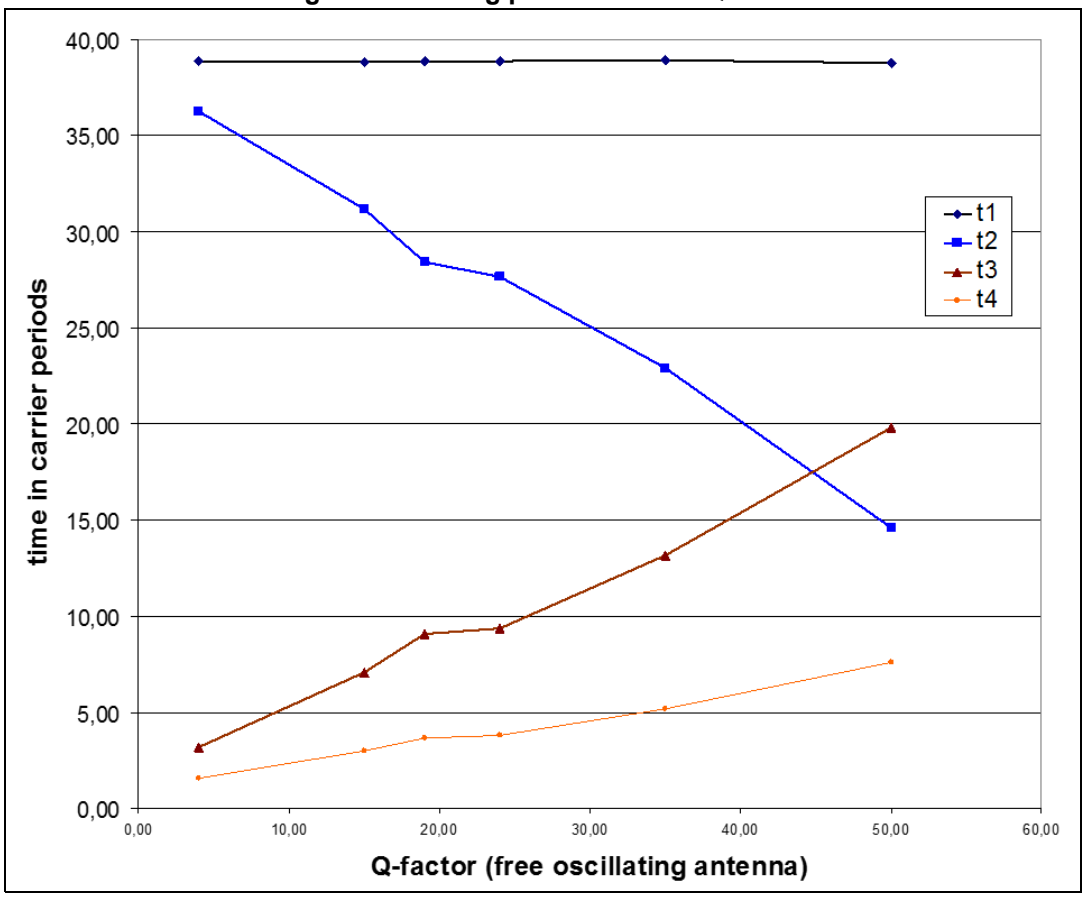


Table 1. Timing parameters for Type-A with 106 kbit/s

Parameter	Condition	Min	Max
t_1	-	6 / fc	40.5 / fc
t_2	t_1 > 34 / fc	7 / fc	t_1
	t_1 ≤ 34 / fc	10 / fc	
t_3	-	1.5 t_4	16 / fc
t_4	-	0	6 / fc

Figure 10. Timing parameters vs. Q factor



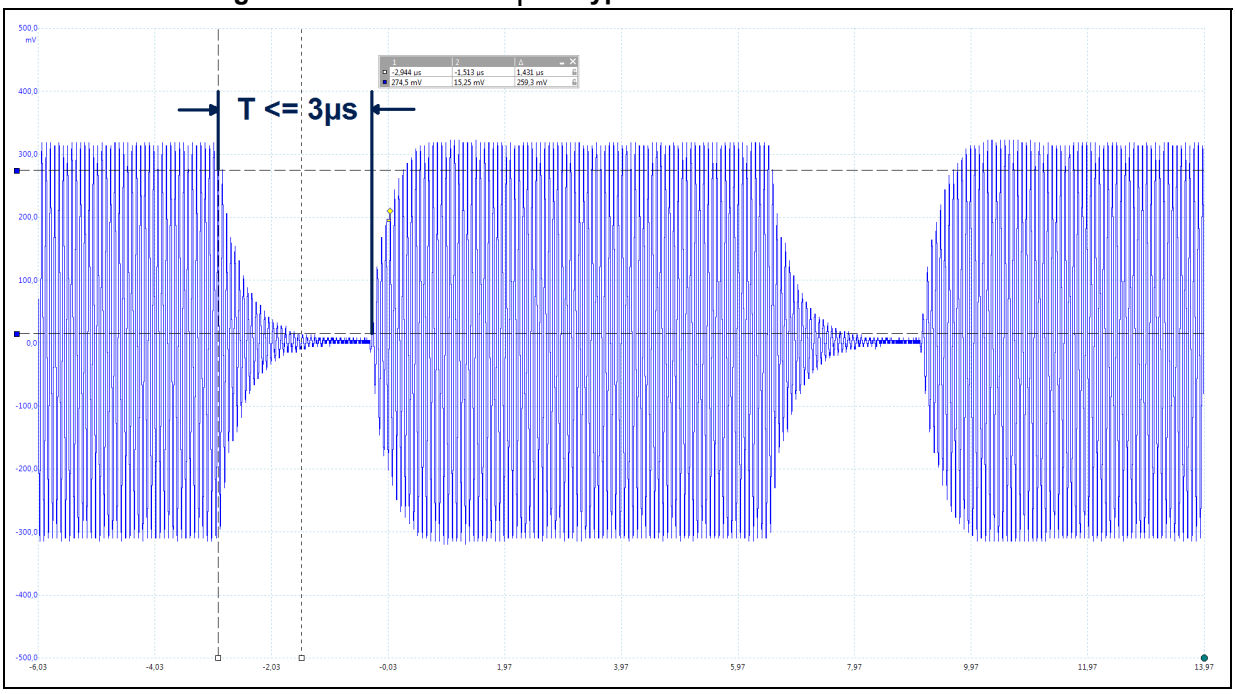
For each protocol (Type-A, Type-B) and data rate a maximum allowable Q factor can be determined, it must not be exceeded to get a modulated signal compliant with ISO waveforms.

The calculation of the maximum allowable Q factor for Type-A with a data rate of 106 kbit/s is based on the bandwidth - time product, and a on definition of the Q factor resulting in the following equation:

$$B * T \geq 1;\ Q = f_{work} / B \rightarrow Q \leq f_{work} * T \rightarrow Q \leq 13.56\ MHz * 3\ \mu s = 41$$

In the above calculation the time T, represented in *Figure 11*, is the highest possible value of the timing parameter t_1 according to the ISO 14443 standard.

Figure 11. Definition of t_1 for Type-A with a data rate of 106 kbit/s



The Q factor for the application must to be below 41 (for Type-A and 106 kbit/s) to achieve standard-compliant rise and fall times, hence the previously calculated Q factor is too high and has to be lowered. This is achieved by connecting an external parallel resistor (R_Q) at the antenna pins. The resistor value depends upon the targeted Q factor (8), and is determined as follows:

$$R_T = Q * \omega * L_{ANT} = 8 * 2\,\pi * 13.56\ MHz * 926\ nH = 631\ \Omega$$

Taking the parasitic resistor R_{PANT} from the antenna equivalent circuit into account, the effective resistor R_Q to adjust the Q factor to 20 is calculated by the formula below

$$R_Q = (R_{PANT} * R_T) / (R_{PANT} - R_T) = (2.76\ k\Omega * 631\ \Omega) / (2.76\ k\Omega - 631\ \Omega) = 818\ \Omega$$

The closest available component value is 820 Ω.

The explanation of how to determine the antenna equivalent circuit and the resistor for the Q factor adjustment is the theoretical background on which the ST25R antenna matching tool is based on.

5 Antenna design

5.1 Boundary conditions and simulation model

The design of a proximity reader system requires a knowledge of the end user application. This includes the environmental conditions when placing the reader or type of cards to be used.

Some basic boundary conditions need to be considered in advance, among them:

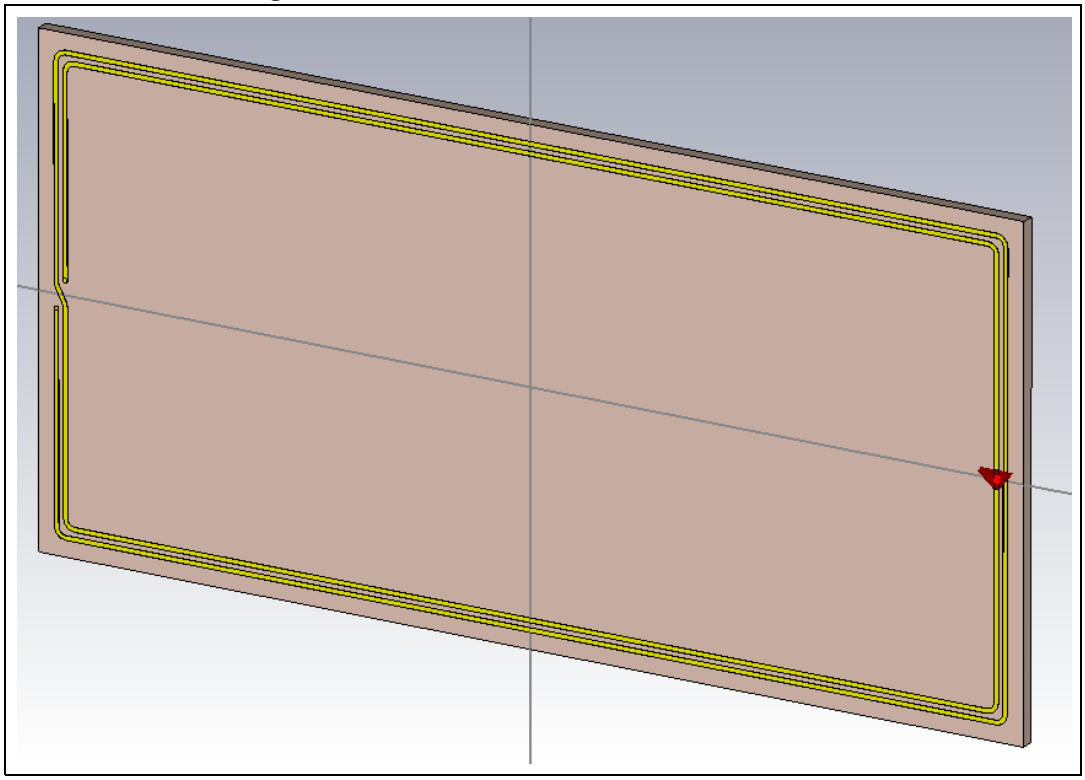
- target reading distance
- tag / card type
- output power
- EMC regulations
- industrial design
- antenna placement
- environmental influences
- supported NFC technologies and standards, and data rates.

The design of an antenna must fit the industrial design of the application, not always there is a large degree of freedom on where to place the magnetic loop. The best case of an antenna placement is far away from electronics or other components like batteries, displays or large ground planes that harm the effective radiated RF field.

As guidelines for the antenna design three antennas of different (but no specific) sizes have been simulated. All of them have a constant number of tracks (two) with a copper thickness of 35 µm on an FR4 plate, with a thickness of 1.5 mm.

Figure 12 shows the EM - simulation model with the biggest size. The simulations have been carried out in the frequency domain.

Figure 12. Simulation model of the coil antenna



To find the dependency of the antenna Q factor and of its other parameters upon the geometry, the trace width and the gap width between traces, as well as the antenna size, have been varied in the simulation.

5.2 Simulation results

The main antenna electrical parameters, as a function of antenna size, trace and gap width, are shown in figures *13* to *17*. *Table 2* summarizes their behavior.

The Q factor depends also upon the antenna size, but the relation is more complex and a more detailed analysis is needed. Additional antenna parameters like inductance, series DC resistance, parallel resistance and self-resonance frequency influence the Q factor, too.

The Q factor of a parallel resonance circuit is:

$$Q = R_{PANT} / (2 \pi f_{carrier} L)$$

where

- R_{PANT} is the total parallel resistance, see *Section 4.3* for details
- L is the antenna inductance
- $f_{carrier}$ is the carrier frequency

The resonance frequency depends on the electrical length of the antenna. The shorter the electrical length, the higher this frequency.

Figure 13. Antenna Q factor vs. antenna size, trace and gap width

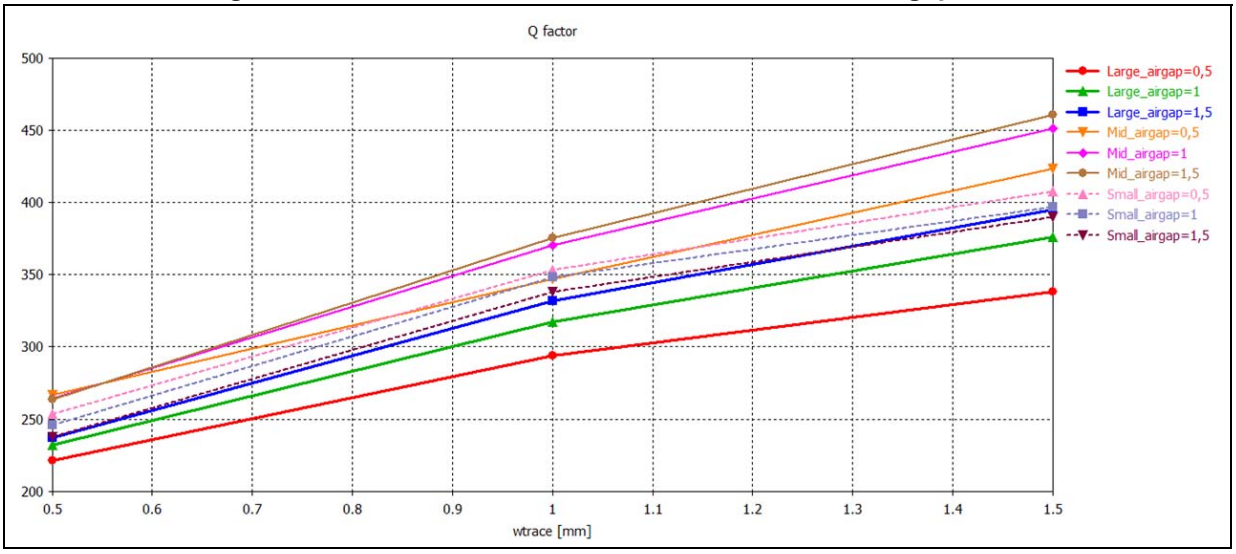


Figure 14. Inductance vs. antenna size, trace and gap width

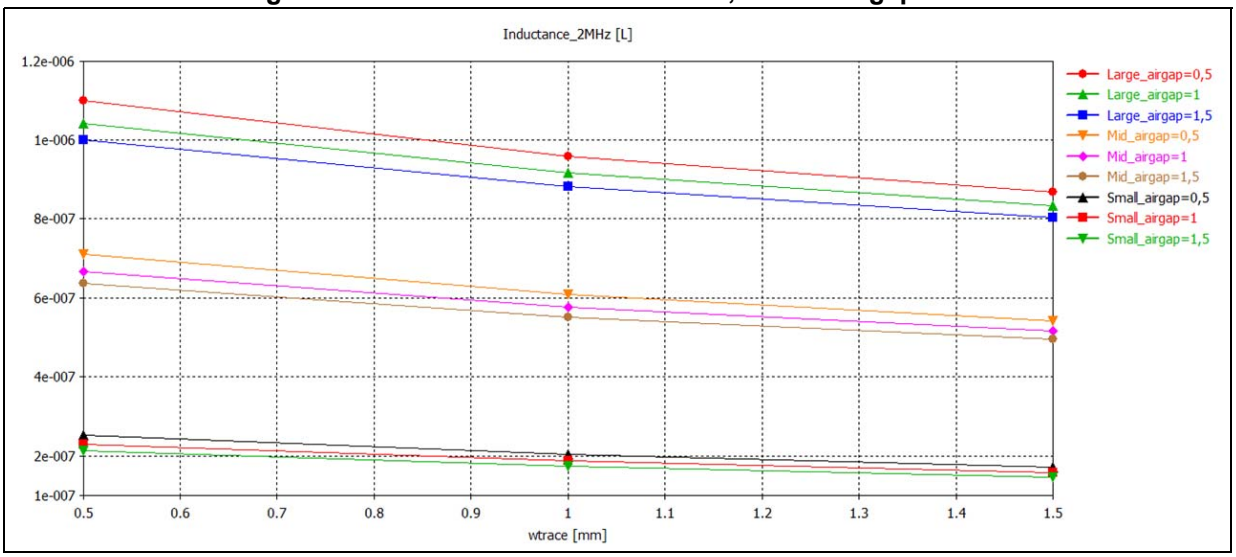


Figure 15. Series DC resistance vs. antenna size, trace and gap width

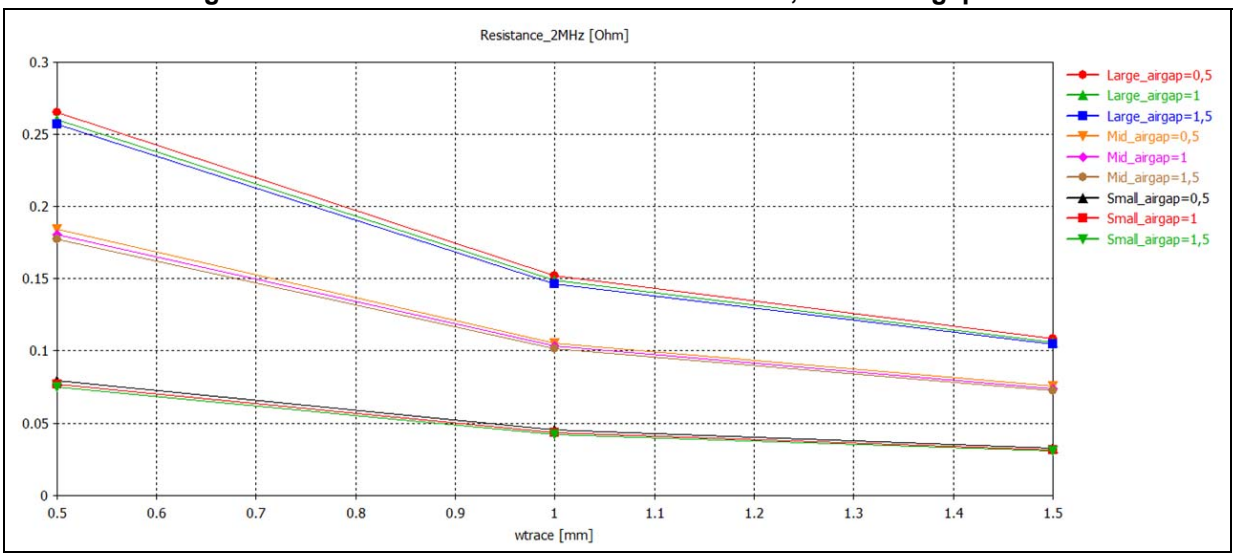


Figure 16. Parallel resistance vs. antenna size, trace and gap width

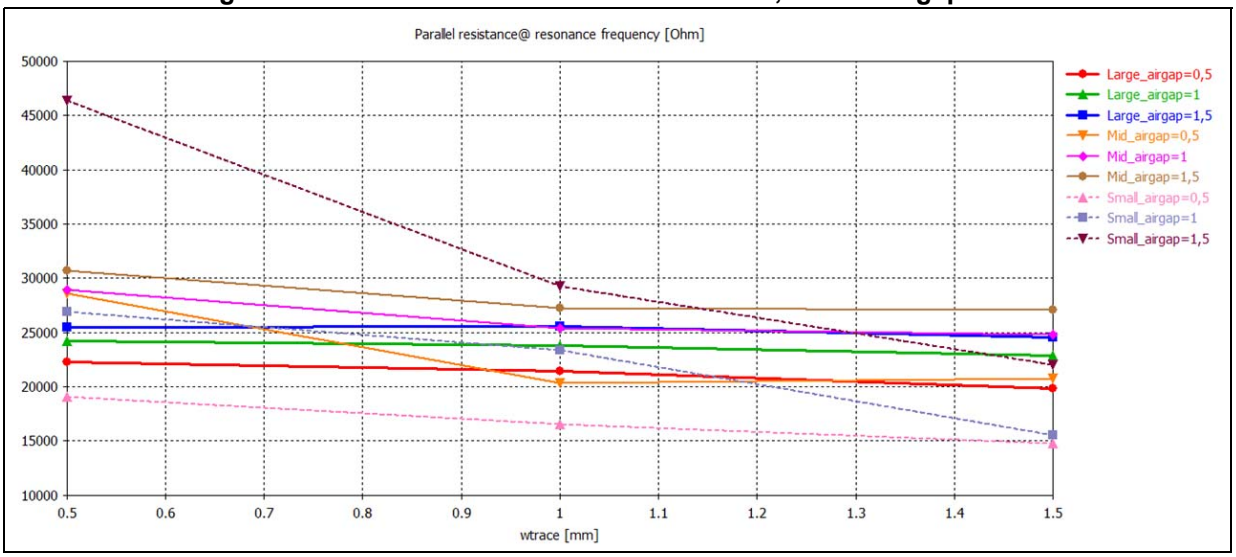


Figure 17. Resonance frequency vs. antenna size, trace and gap width

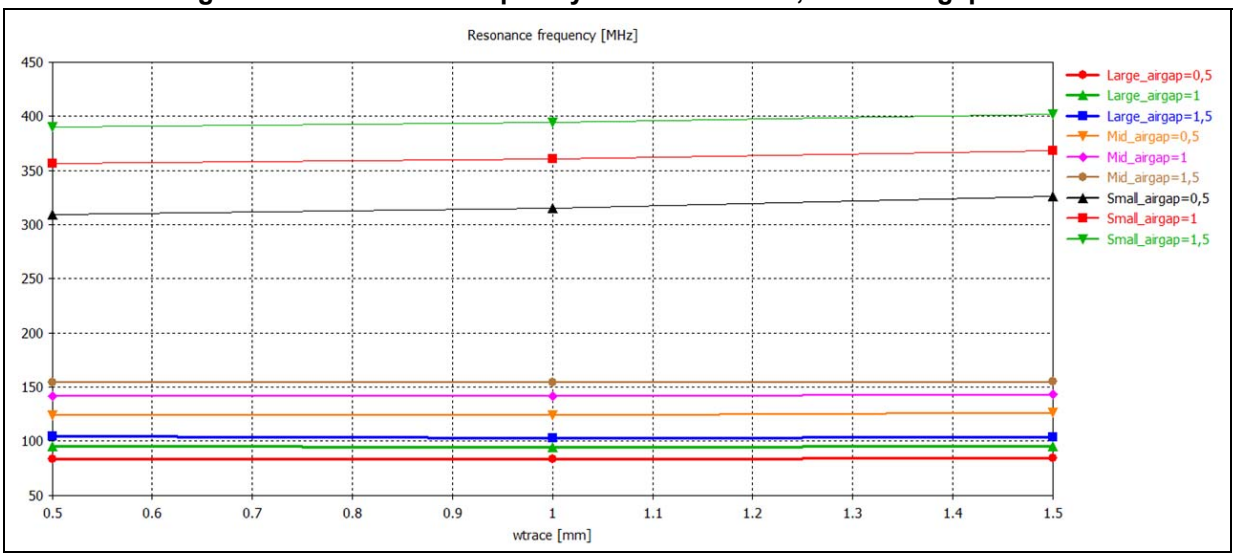


Table 2. Behavior of antenna parameters vs. geometrical parameters

Parameter	Action	Effect on parameter	Q factor
Q factor	Increase trace width	-	Increases
	Increase gap width		
Inductance	Larger antenna	Increases	Decreases
	Decrease trace width		
	Decrease gap width		
Series DC resistance	Larger antenna	Increases	Decreases
	Decrease trace width		
	Decrease gap width		
Parallel resistance	Decrease trace width	Increases	Increases
	Increase gap width		
Resonance frequency	Smaller antenna	Increases	Increases
	increase gap width		

Note: The separated view of each antenna parameter is a theoretical one to understand the basic behavior. In reality all parameter are linked together, e.g. if the inductance is increased by a larger antenna (lower Q), the electrical length increases, which in turn lowers the resonance frequency (Q increases) and the series DC resistance increases (lowering Q).

The inductance of magnetic loop antennas is defined by the electrical length of the conductor. The longer and thinner the way the signal has to travel (more electrical length) the higher the inductance of the coil. On the other hand the wider and shorter a transmission line is the more capacitive its behavior. Changing the inductance of a loop antenna may thus be realized by altering the thickness of the turns, the gap width or the size of the antenna.

A value to be targeted in loop antenna design for NFC reader applications is in the 200 to 1500 nH range. Depending on the application higher inductance values can be chosen and are supported by the chip.

In direct relation to the change of the inductance stands the series resistance of the loop antenna, which increases with longer and thinner turns. The antenna self-resonance frequency shows the tendency to increase with larger gap widths between the antenna tracks and also with decreasing size of the antenna.

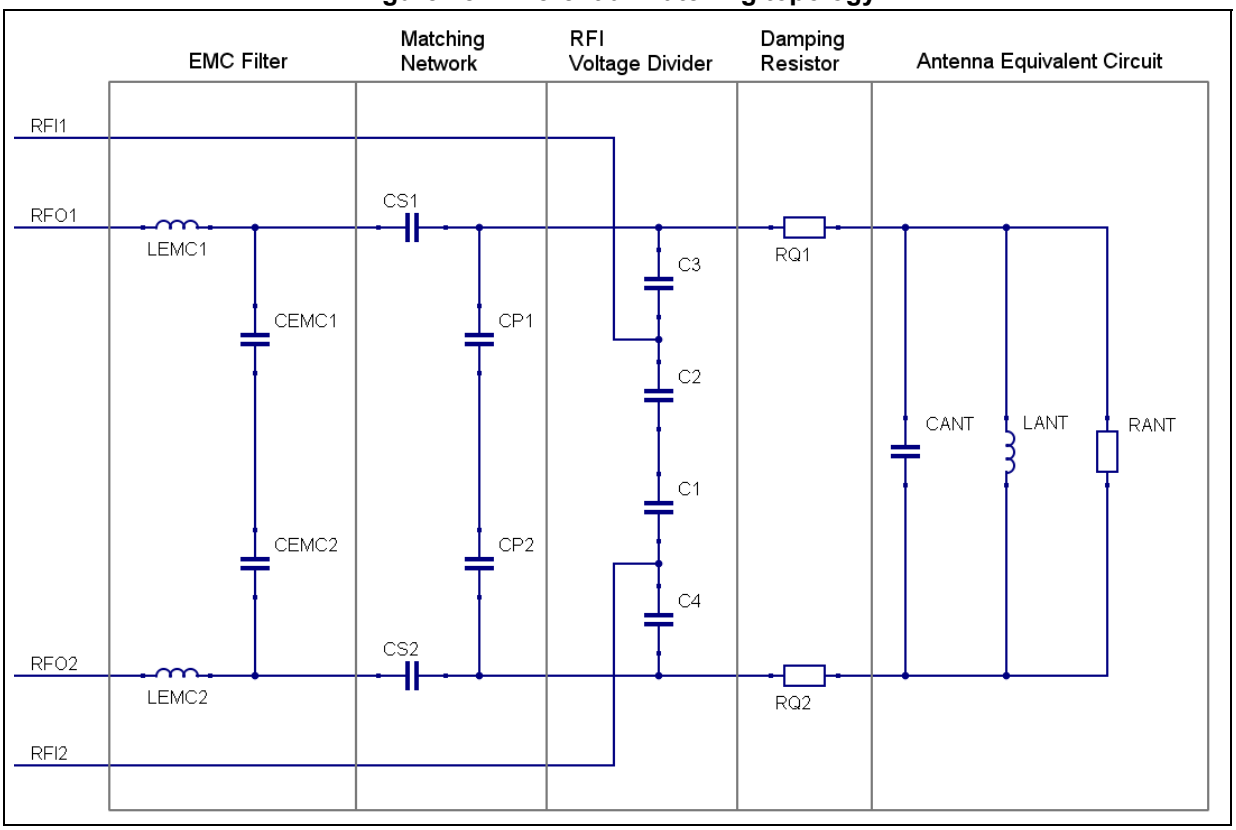
As mentioned in *Section 5* the antenna has to be designed with a Q factor higher than the one needed for the application. The reason is that the Q factor can be decreased by a damping resistor connected at the antenna pins, but it cannot be increased anymore, except with a redesign of the antenna.

6 Antenna matching

The whole antenna interface stage consisting of EMC filter, matching network, RFI voltage divider and antenna equivalent circuit together with the resistor for the Q factor adjustment is represented in *Figure 18* as a differential topology.

The EMC filter is a one stage filter made up of a series inductor and a parallel capacitor to ground. The matching network consists of a series and a parallel capacitor, whereas just one parallel component is used in this topology. The resistor for the Q factor adjustment is a series resistor. The antenna is shown as an equivalent circuit consisting of a series inductor, a parallel resistor and a parallel capacitor. The voltage divider for the receive path is capacitive and connected directly at the antenna pins.

Figure 18. Differential matching topology



6.1 Matching tool

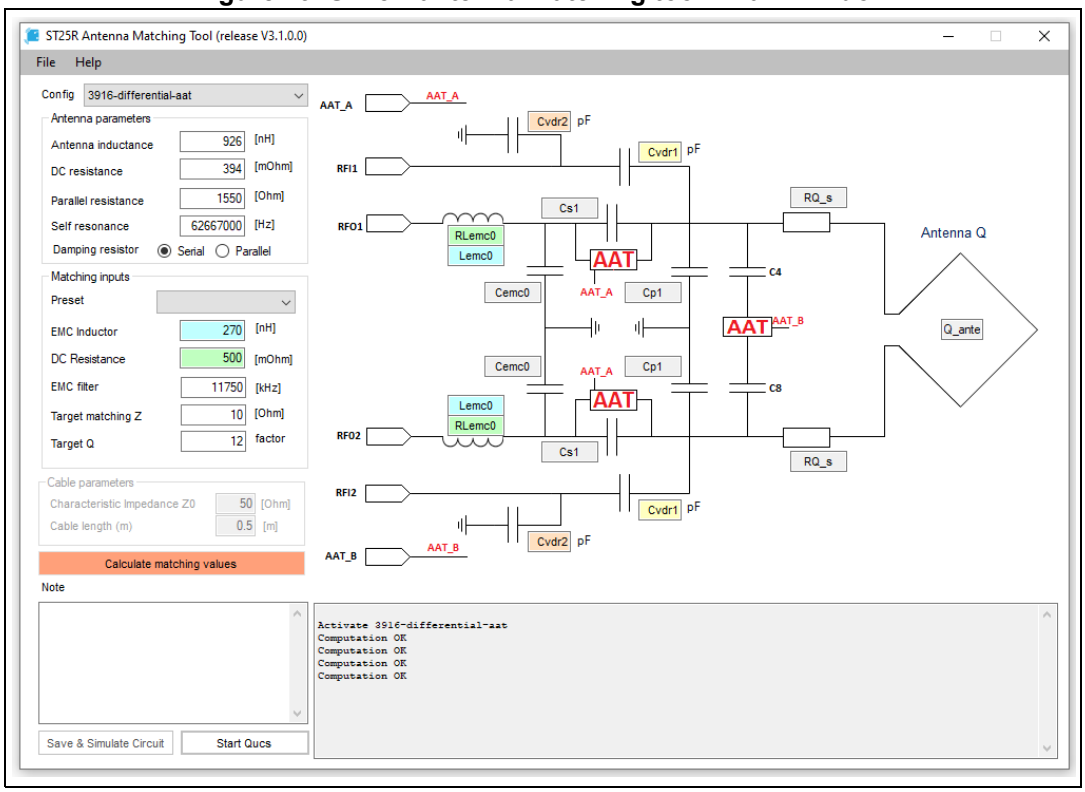
The STMicroelectronics ST25R antenna matching tool is a straightforward tool to determine the matching for the antenna once the electrical antenna parameters have been measured. The tool comes with an intuitive GUI to guide the user through the process of finding the component values. Additionally, a program called Qucs Circuit Simulator can be started directly from the GUI. The Qucs simulation tool can be used to perform AC, S-Parameter and Transient simulations to verify the component values.

Qucs is integrated into the ST25R antenna matching tool installer, and can also be freely downloaded at http://sourceforge.net (it is recommended to use version number 0.0.18, the one embedded into the ST25R antenna matching tool). As for the installation path, do not use the default Windows directory, but rather a path like C:\Tools\Qucs.To open the matching tool, download the executable (STSW-ST25R004) from *www.st.com*. The main window is shown in *Figure 19*.

The process flow is from top to bottom, made up of five basic steps

1. Insert the measured antenna input parameters at 1 MHz and SRF
2. Select a precondition, or define your own condition
3. Define EMC filter coil inductance and DC resistance
4. Enter the target matching impedance and target Q factor
5. Calculate and simulate the computed values

Figure 19. ST25R antenna matching tool - Main window



The first step is already completed in *Figure 19*: as described in *Section 4.2* the antenna parameter have already been entered in the input parameter fields.

In the precondition tab enter the desired EMC filter cutoff frequency, the target matching impedance and the desired antenna Q factor. There are three preconditions defined, either select one of them or define your own condition, depending on the application.

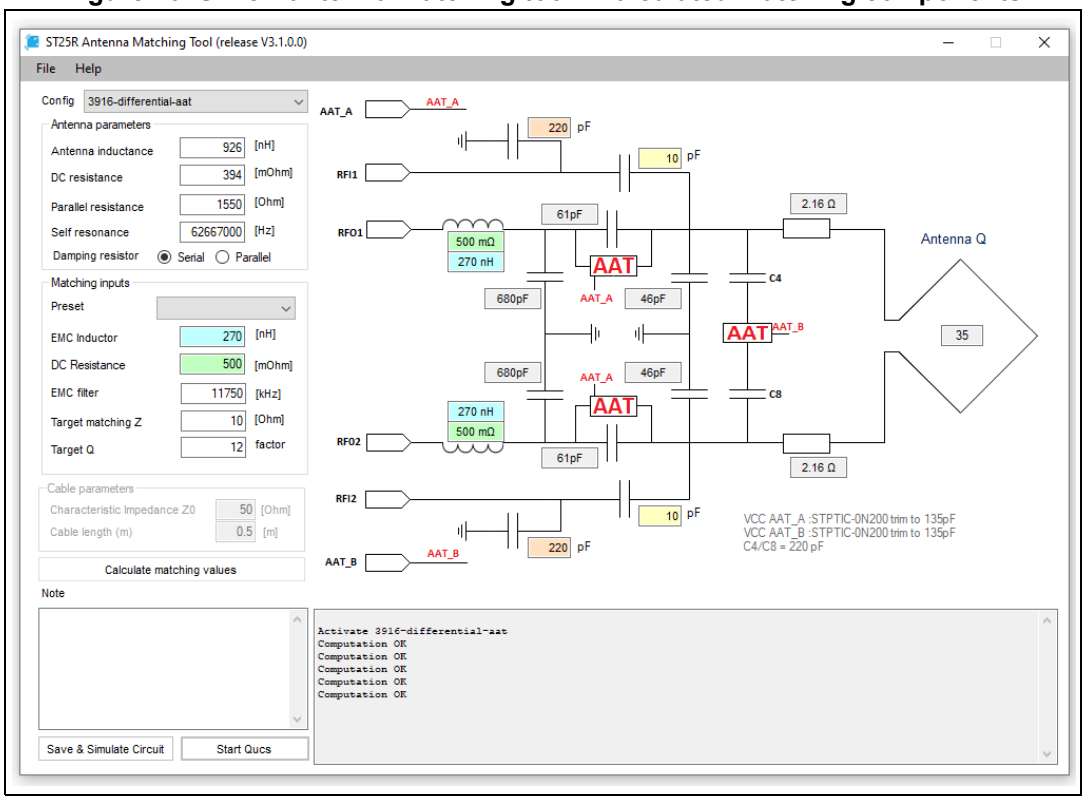
The third step is to choose a value for the inductance of the EMC filter.

The selected EMC filter frequency and inductance are dependent on each other and may have to be adapted. The EMC filter capacitor value is calculated from these two inputs. Depending on the chosen EMC inductors, a proper inductor DC resistance has to be

entered. This value can be found in the datasheet of the inductor. The antenna Q factor is shown after the computation in the schematic area. If the desired Q factor is higher than the calculated antenna Q factor, a negative damping resistor value is displayed.

By clicking the “Calculate” button all the component values are calculated and shown in the schematic part (*Figure 20*).

Figure 20. ST25R antenna matching tool - Calculated matching components



Parasitic (like ESR of the capacitors) and special component parameters are not taken into account.

With all values calculated the results can now be simulated: click on Simulate Circuit, a save dialog pops up asking to save the schematic file. Carefully choose the data destination (depending on the r/w permissions), the suggested location is

`%userprofile%\.qucs\PROJECT_prj (PROJECT = Project Name; _prj = QUCS suffix)`

If the schematic files need to be loaded to continue the simulations, Qucs can be started by pressing the “Start Qucs” button. If the files are saved in above mentioned location, Qucs automatically finds and displays them in the projects panel.

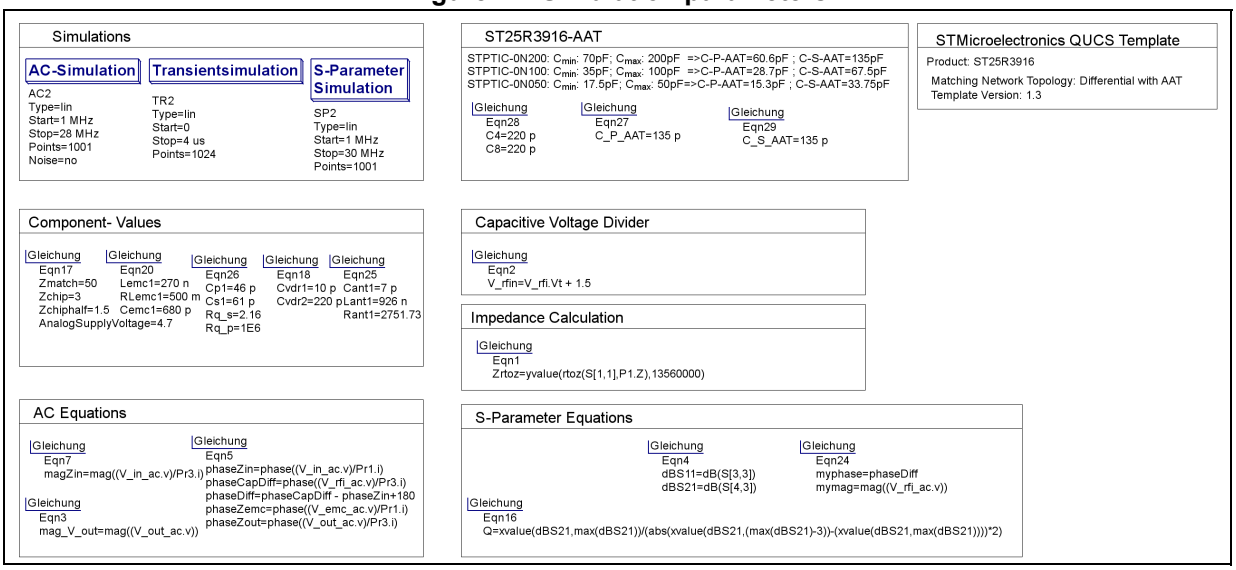
6.2 Simulation

If Qucs has been started via the “Simulate Circuit” button and the schematic files have been saved accordingly, Qucs automatically loads the schematics. If this does not happen, use the file-open dialog to load the schematics.

Qucs uses a schematic file to setup the simulation and a display file for the results. The before-calculated values are automatically inserted in a Qucs schematic template, displayed while saving.

The component values and simulation parameters are found in the top section of the sheet, which also contains formulas required for the display file/view. It is strongly recommended to change component values only in the section “Component-Values” and not in the simulation model itself. *Figure 21* shows the antenna parameters, very similar to the before-calculated values.

Figure 21. Simulation parameters



6.2.1 Models

Three models are used to perform simulations:

1. S-parameter model (*Figure 22*) is used to calculate the target matching impedance in the Smith chart. 50 Ω is used as source impedance to compare the results with the VNA. The results are shown in *Figure 25*.
2. Transient simulation (*Figure 23*) checks the waveform of the OOK and calculates the RFI Voltage to define the capacitive voltage divider values. The estimated IC output driver impedance of 2 Ω is used. The results are shown in *Figure 27*.
3. AC simulation (*Figure 24*) calculates the reflection and transmission coefficients (S11 and S21) with the IC output driver impedance of 2 Ω. This is used to calculate the Q factor, the phase differences between RFO and RFI and to monitor the relation between the resonance frequencies of the antenna and EMC filter stages. The results are shown in *Figure 25* and *Figure 27*.

Figure 22 shows the S-Parameter model, while “Component-Values” and “Antenna-Trim” areas are shown in *Figure 21*. The values assigned here are automatically linked to all three models.

The difference between S-parameter and AC model is the impedance of the power source.

While measuring the impedance (S-parameter measurement) the matching network and antenna is powered by this VNA. The impedance of the VNA is in most cases 50 Ω, therefore the source impedance of the S-parameter model has to be 50 Ω.

Note: The AAT circuitry from the simulation tool is not applicable for the ST25R3916. The ST25R antenna matching tool is a general tool that can be used with different HF reader ICs.

The transient model is powered by two periodic rectangular voltage pulse sources. Every source represents one single ended driver stage. The output resistance of the driver stage can be defined by setting Z_{RFO}.

The AC model is used to simulate the matching network during normal operation, hence the source impedance of the AC power source must correlate with the chip impedance. The forward reflection (S11) and forward transmission coefficients (S21), as well as the phase and magnitude characteristics can be calculated with this simulation. At the end, the results are displayed in a new tab. It is also possible to include further simulations, like parameter sweep.

Figure 22. S-parameter model

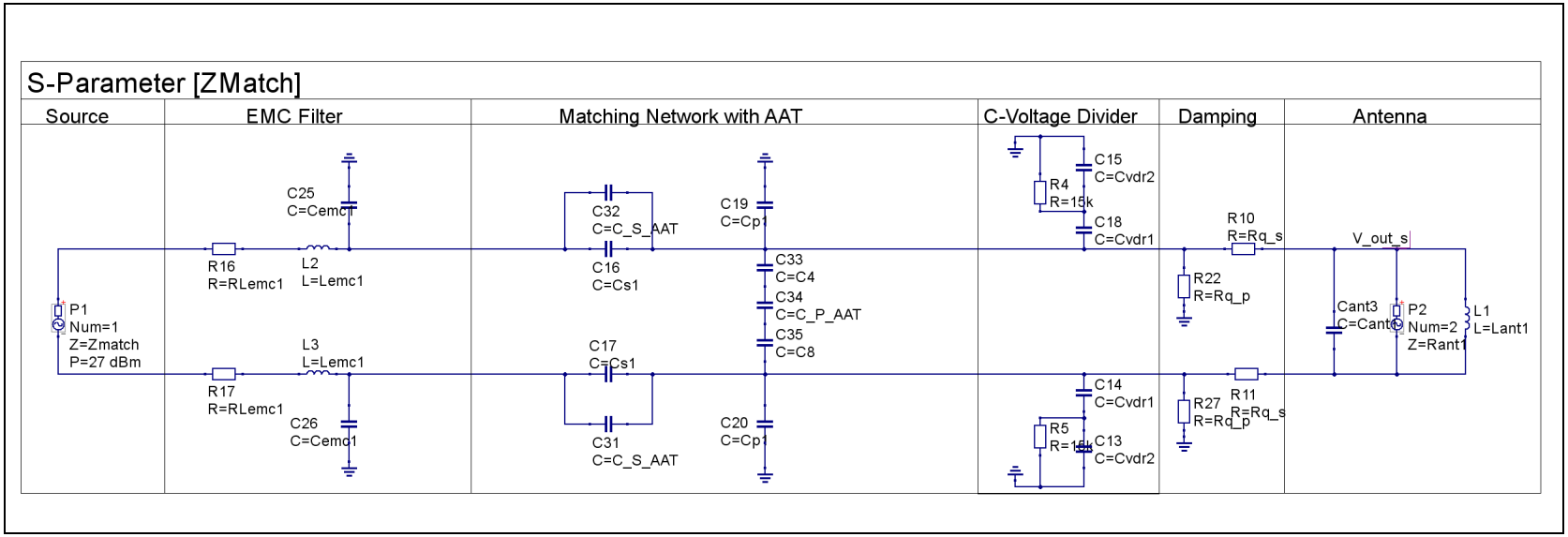


Figure 23. Transient simulation

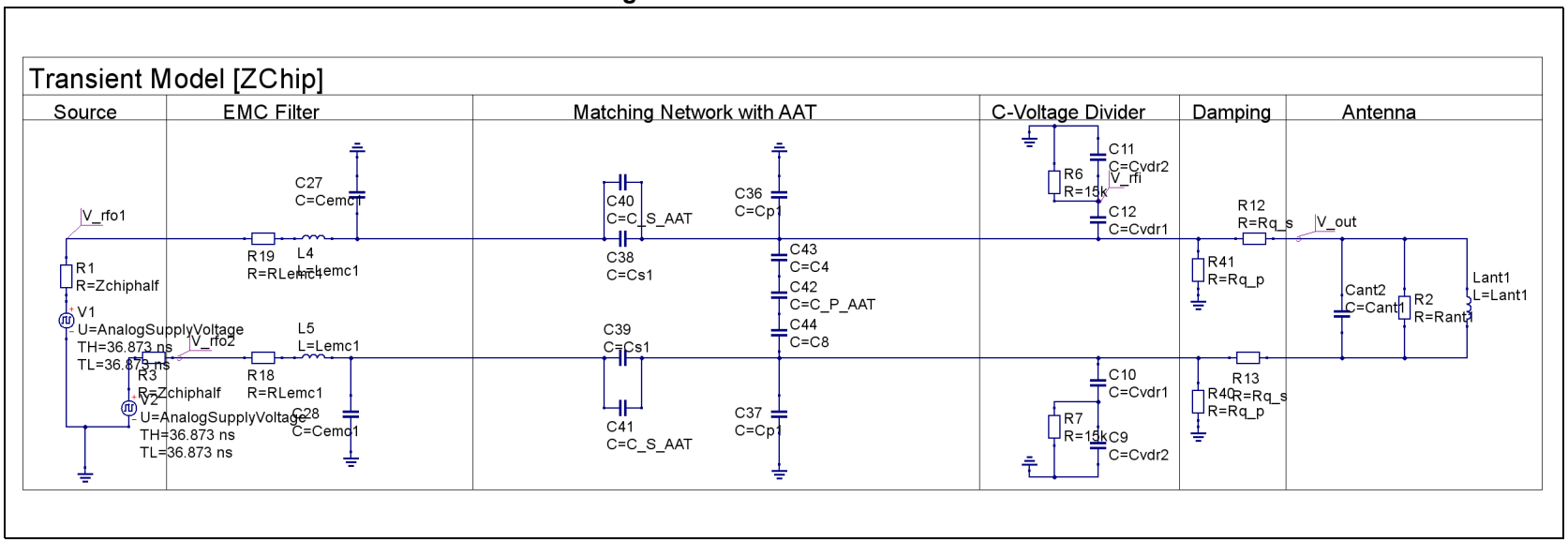
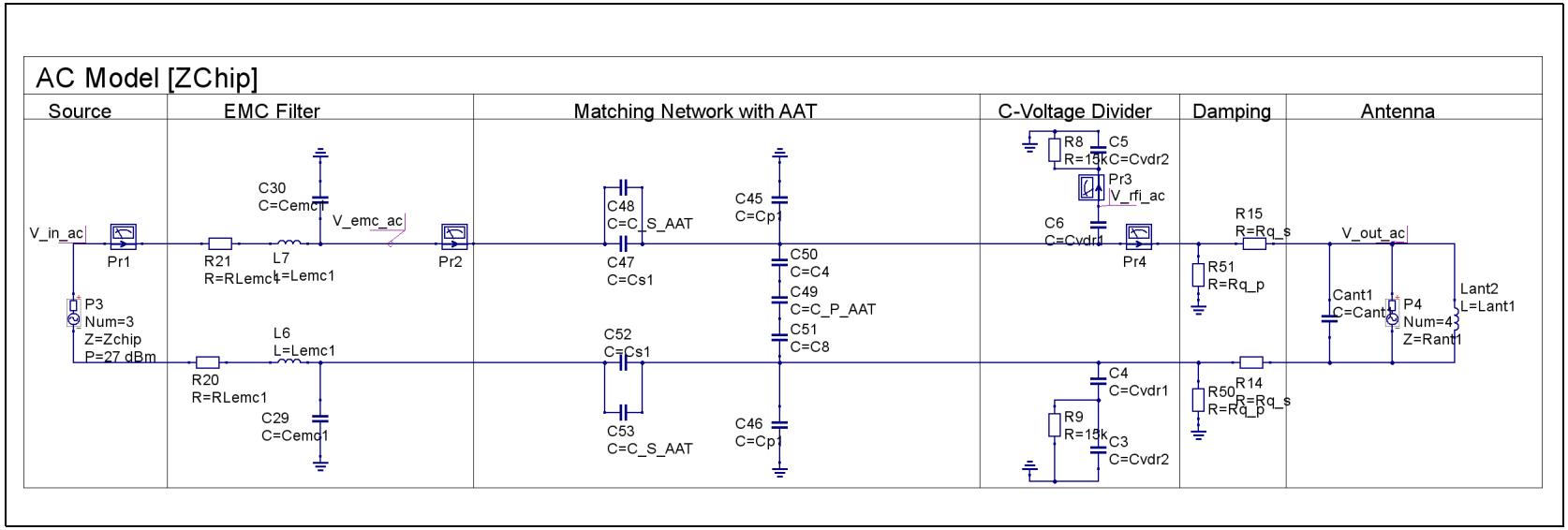


Figure 24. AC simulation

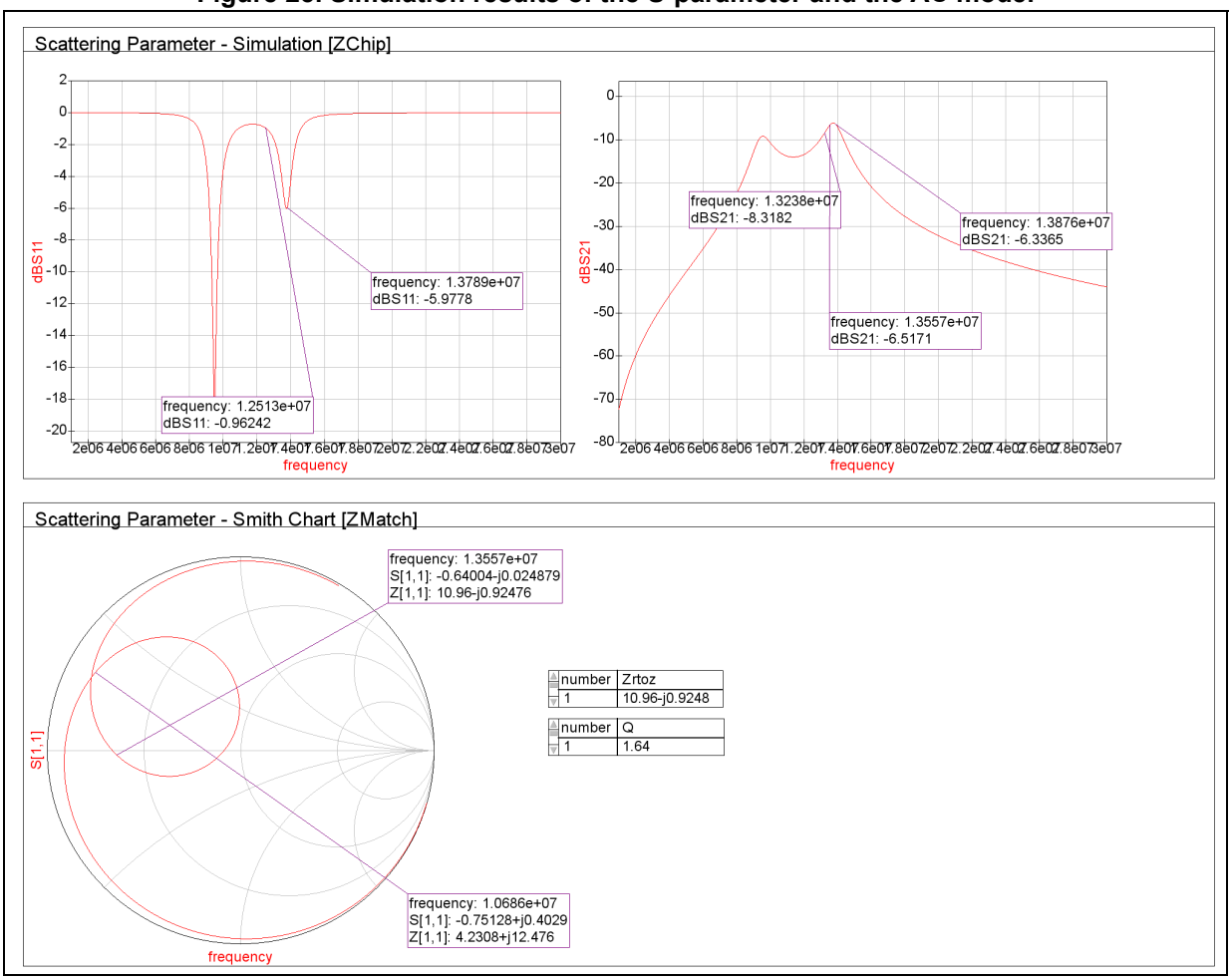


6.2.2 Results

The transfer functions dB [S11] and dB [S21] are calculated in Eqn4 (S-Parameter Equations box in *Figure 21*). This equation uses port 3 and 4 of the AC simulation model, dB [S11] represents the reflected power on the RFOx pins. With better matching between ST25R3916 driver stages and matching network, less power is reflected. In our case the output resistance is set to 2 Ω differential and the matching network is tuned to (10.96 – j 0.9248) Ω.

Figure 25 shows the forward transmission, which evidences the damping over frequency. The Smith chart displays the nominal resistance of the matching network plus antenna over frequency. If the curve cuts the real axis the imaginary part is zero and the circuit is in resonance. In the case under consideration one resonance frequency of the matching network is at 13.57 MHz. The complex resistance of the circuit at this frequency is (10.96 – j 0.9248) Ω. Because the nominal resistance is 50 Ω, this graph has to match with the measurement of the VNA.

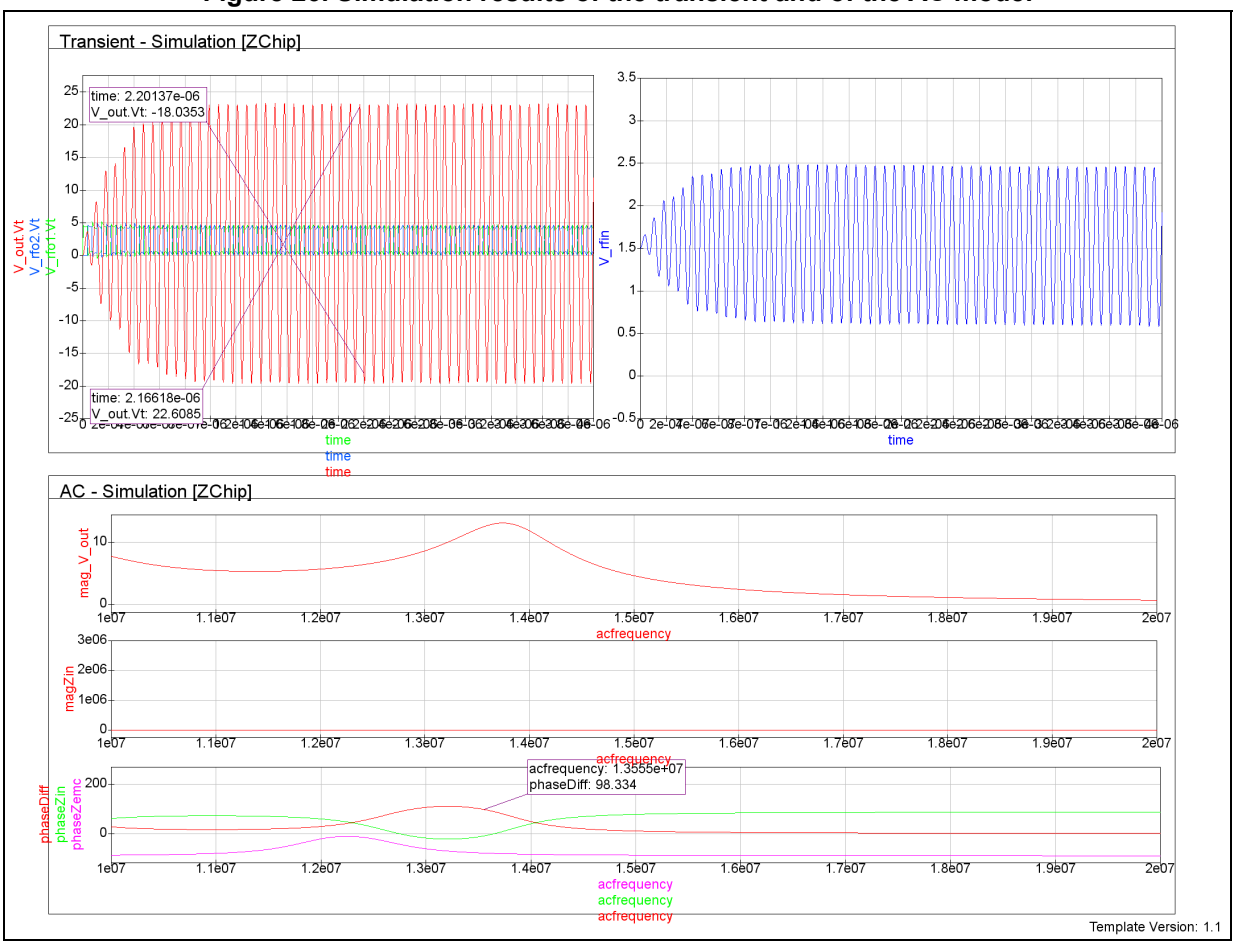
Figure 25. Simulation results of the S-parameter and the AC model



The Q factor simulation is calculated from the dB[S21] result.

As result of the transient simulation we can have a look at the shaping of the antenna voltage and the voltage at the RFIx pins. Eqn2 (Capacitive Voltage Divider box in *Figure 21*).describes how the voltage at RFIx pins gets biased to the level of AGD (the analog reference voltage). The input voltage must not exceed 3 V_{PP}. In the lower section of *Figure 26* the magnitude of the antenna voltage and matching impedance as well as the phase difference (phasediff) between RF0x and RFIx pins are displayed.

Figure 26. Simulation results of the transient and of the AC model



6.3 Matching network behavior

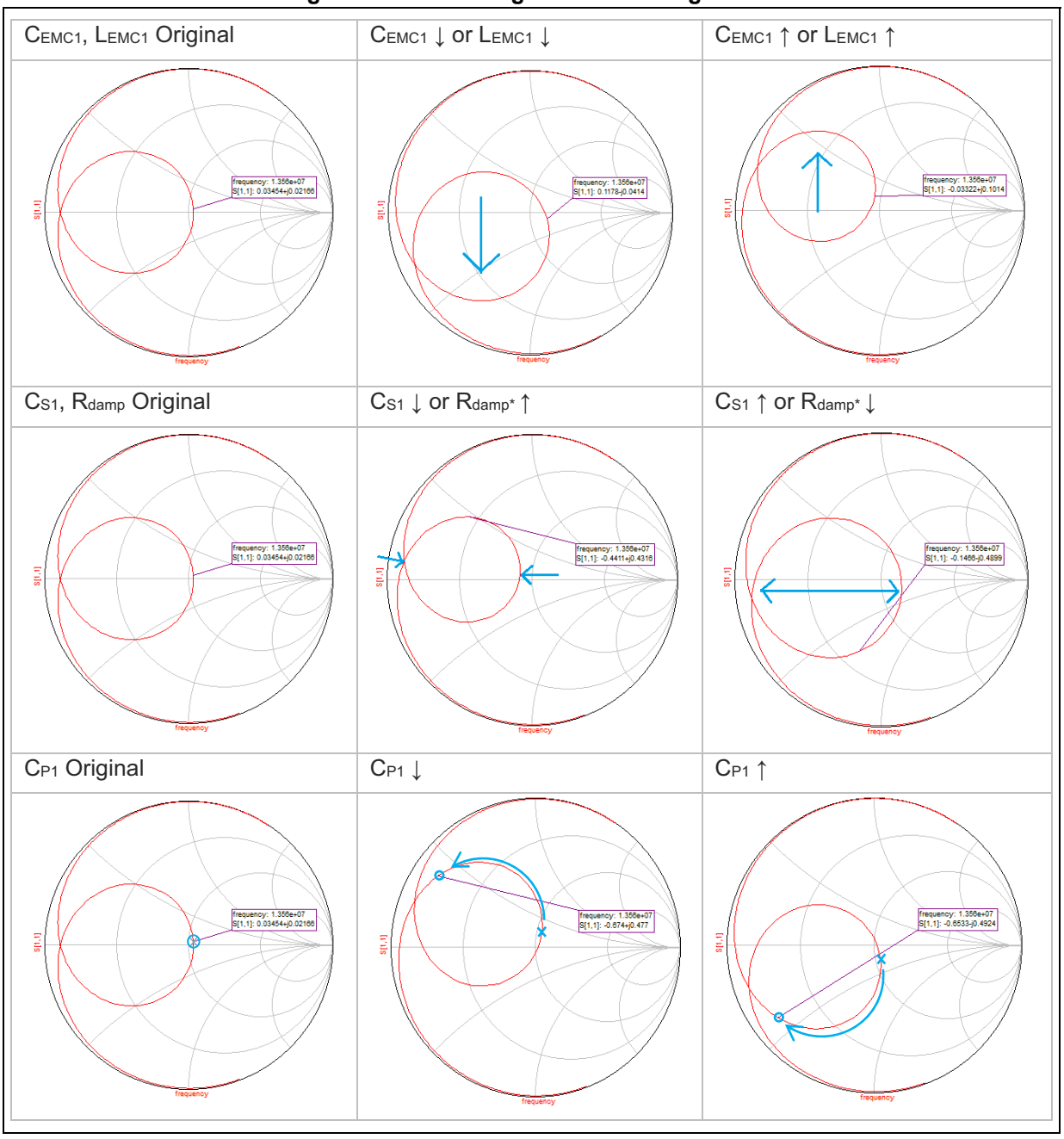
Since the simulation does not always match with the reality, some fine tuning may be needed.

Figure 27 shows how the matching network behaves when some components are changed.

Note that the behavior of R_{damp} is valid only for the series resistor configuration, for the parallel damping resistor the behavior is the opposite.

When changing one component other effects may appear. As an example, changing the serial capacitor changes the diameter of the resonance cycle, but also shifts the resonance frequency, similarly as when changing the parallel capacitor.

Figure 27. Fine tuning of the matching circuit



7 Design verification

This section discusses the verification of the designed antenna and explains the measurement of timing parameters, Q factor, and target matching impedance.

7.1 Measurement of PCD RF analog parameters

To ensure correct operation and interoperability of a reader system, all measurements must be performed according to the required standard (e.g. ISO 14443, or EMV contactless). As an example, to test against ISO 14443 contactless standard it is necessary to use the ISO reference PICC defined in ISO/IEC 10373-6.

Verifying the RF signaling parameters with an oscilloscope loop only gives a first indication on signal forms, but does not produce any meaningful or comparable measurement result.

Figure 28, *Figure 29*, and *Figure 30* show, respectively, snapshots of Type A 106 kbit/s, Type B 106 kbit/s and FeliCa™ measurements with a reference PICC.

Figure 28. ISO 14443 Type A wave shape measurement

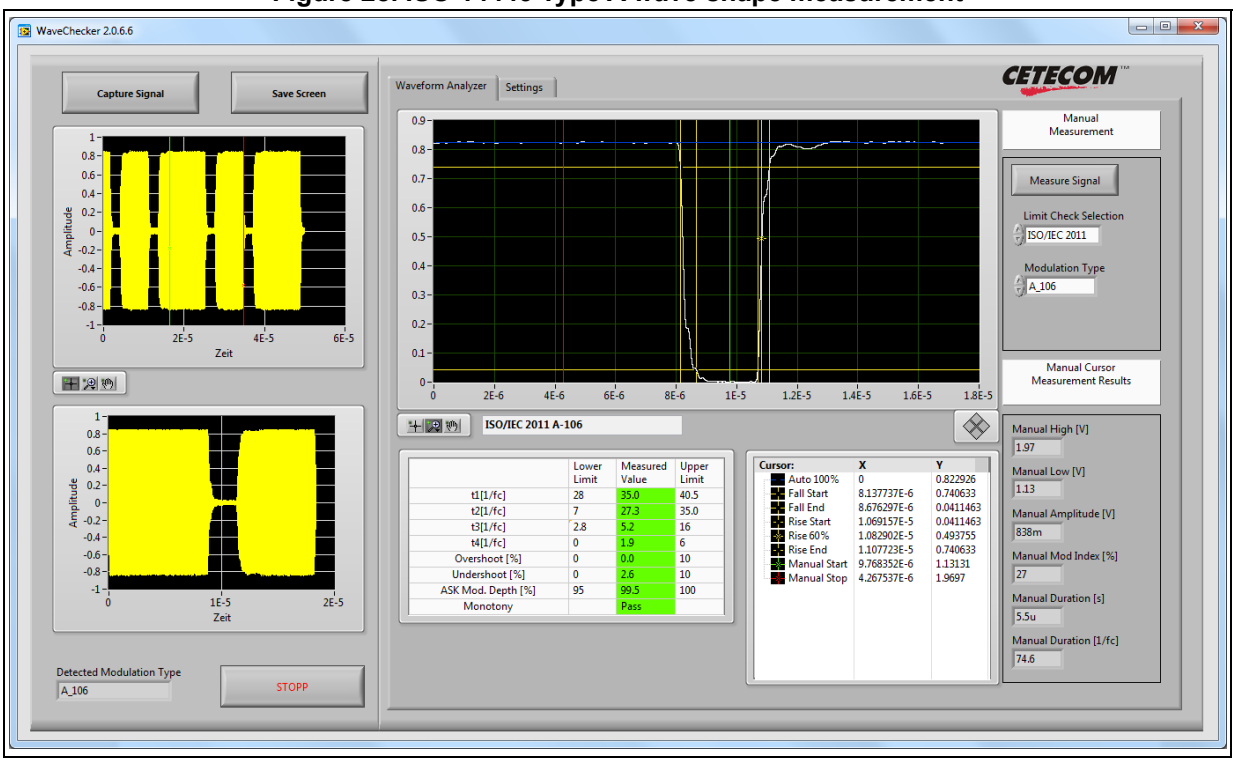


Figure 29. ISO 14443 Type B wave shape measurement

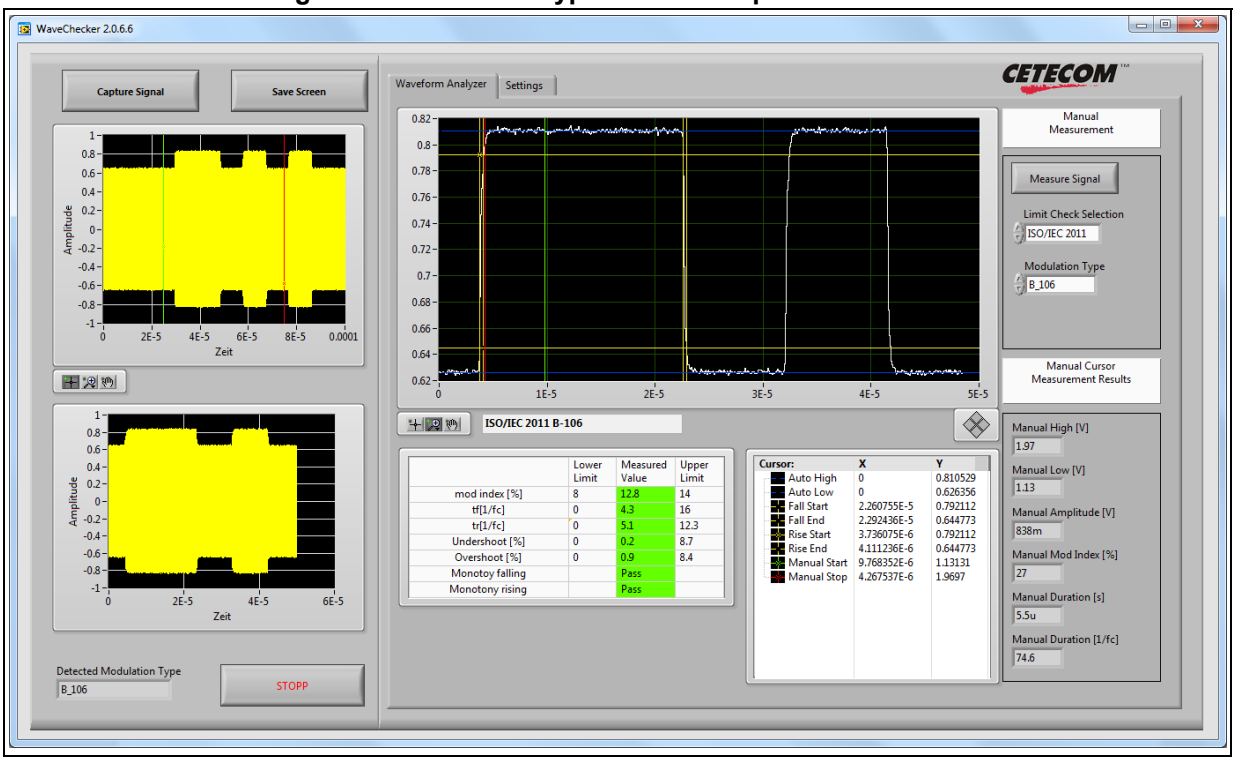
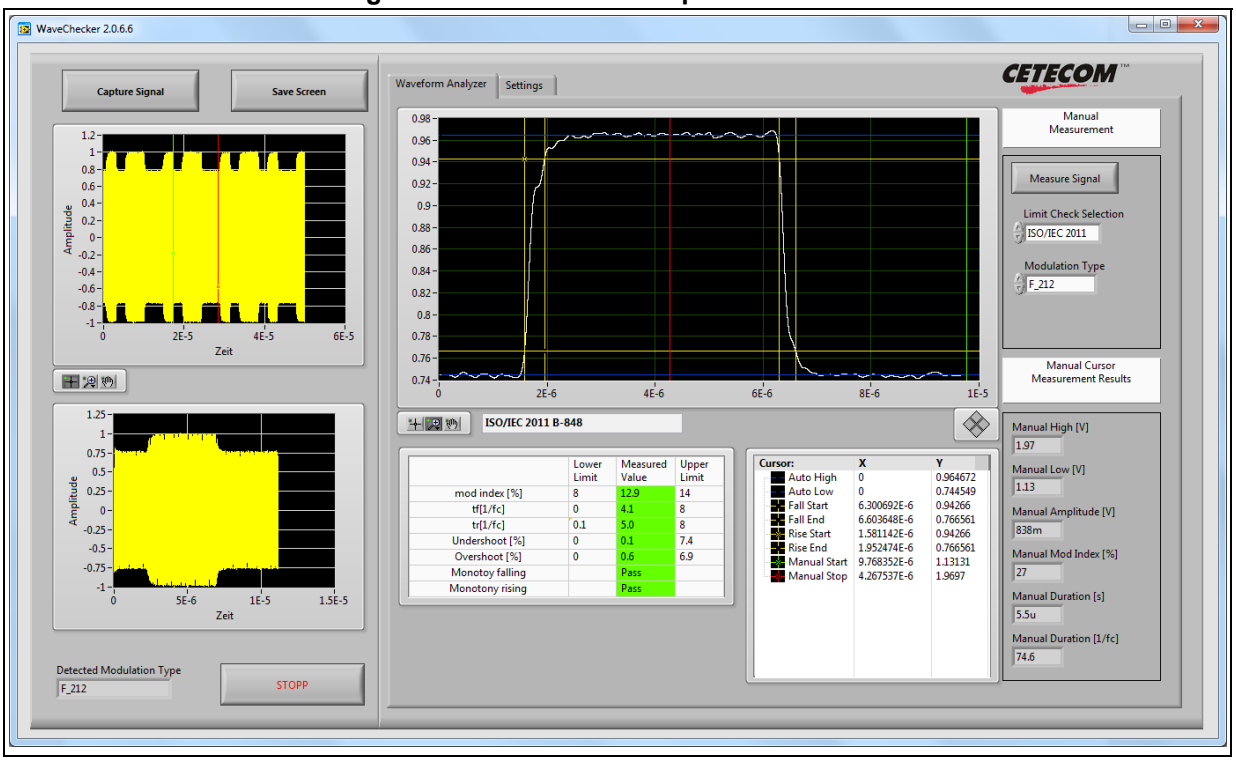


Figure 30. FeliCa wave shape measurement



7.2 Verification of the Q factor in the time domain

The resonance circuit envelope can be calculated (for falling and rising edges) with exponential functions:

$$Q_f = 2 \pi f_{work} [(t_1 - t_2) / (\ln 0.9 - \ln 0.05)]$$

$$Q_r = 2 \pi f_{work} [t_3 / (\ln 0.9 - \ln 0.05)]$$

The overall Q is determined averaging Q_f and Q_r, that is $Q = (Q_f + Q_r) / 2$

7.3 Verification of the Q factor in the frequency domain

The Q factor can be measured using a vector network analyzer and an ISO10373-6 Class 1-3 calibration coil. The sequence is made up of the following steps:

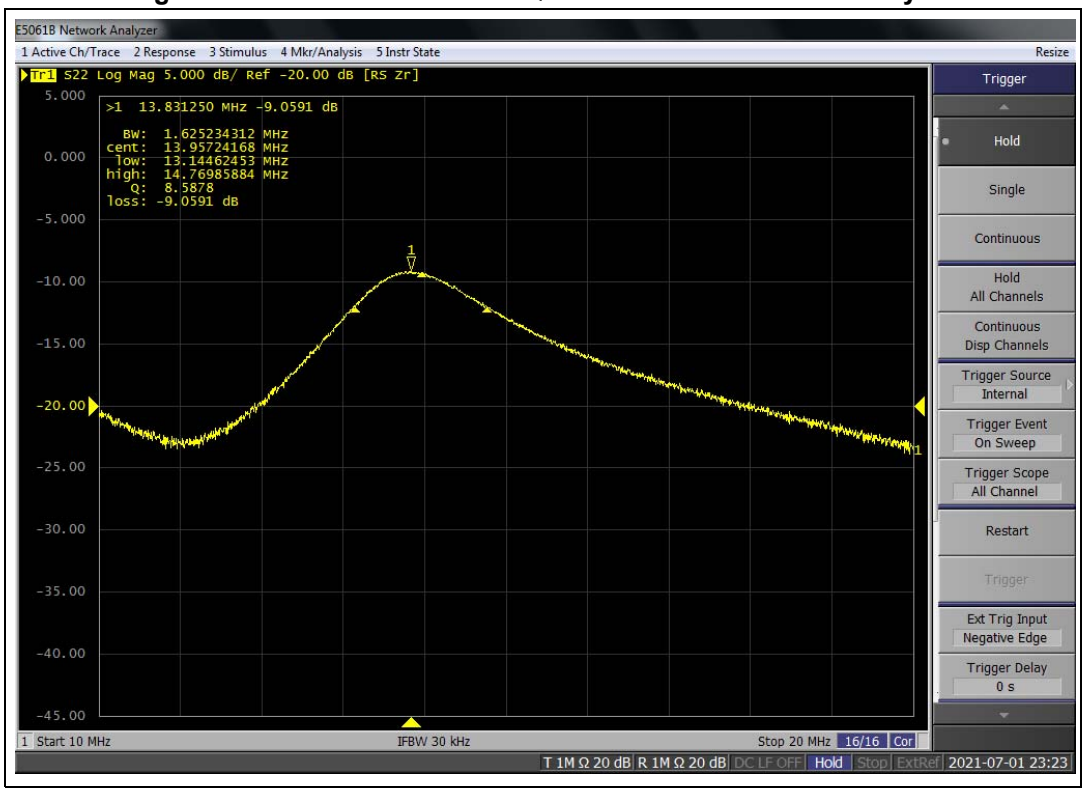
1. Calibrate the network analyzer for a frequency sweep in the 10 to 20 MHz range
2. S11 measurement must be displayed in log mag format.
3. Connect the calibration coil to the VNA.
4. “Short” calibration of the coil and conversion to “Z: Reflection”.
5. Set marker 1 and enable the bandwidth / Q factor measurement.
6. Place the PCD antenna on the measurement coil.

Note: If the reader is plugged and powered, ensure that the TX driver is set to high-Z to avoid an high power transfer to the VNA ports, which can damage the VNA.

7. Place a 2 Ω resistor between the RFO pin to simulate the chip resistance during operation.
8. Press “max search” to align the marker on the resonance frequency peak of the PCD antenna.

Figure 31 shows the results of the measurement.

Figure 31. Measurement of the Q factor with the network analyzer



7.4 Measurement of the target matching impedance

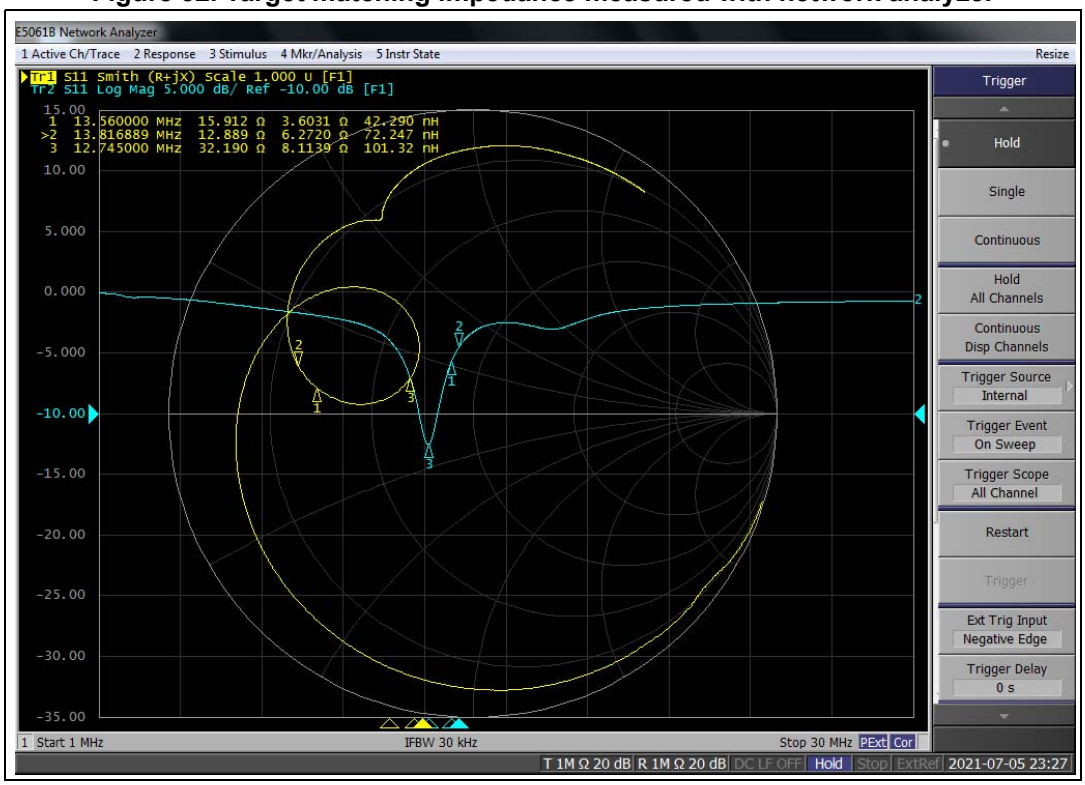
The matching impedance of a reader system must be measured with the antenna placed in its final position. A network analyzer is required and must be configured as described in *Section 4.1*.

Note: If the reader is plugged, ensure that register 0x28 is set to 0xF to avoid high power transfer to the VNA ports.

The target matching impedance is measured differentially.

The results of this measurement (see *Figure 32*) compare nicely with the simulation results.

Figure 32. Target matching impedance measured with network analyzer



7.5 NFC tuning circuit calculation

The NFC tuning circuit calculator applies to ST25R readers. It provides the component values of the matching network for a given NFC antenna.

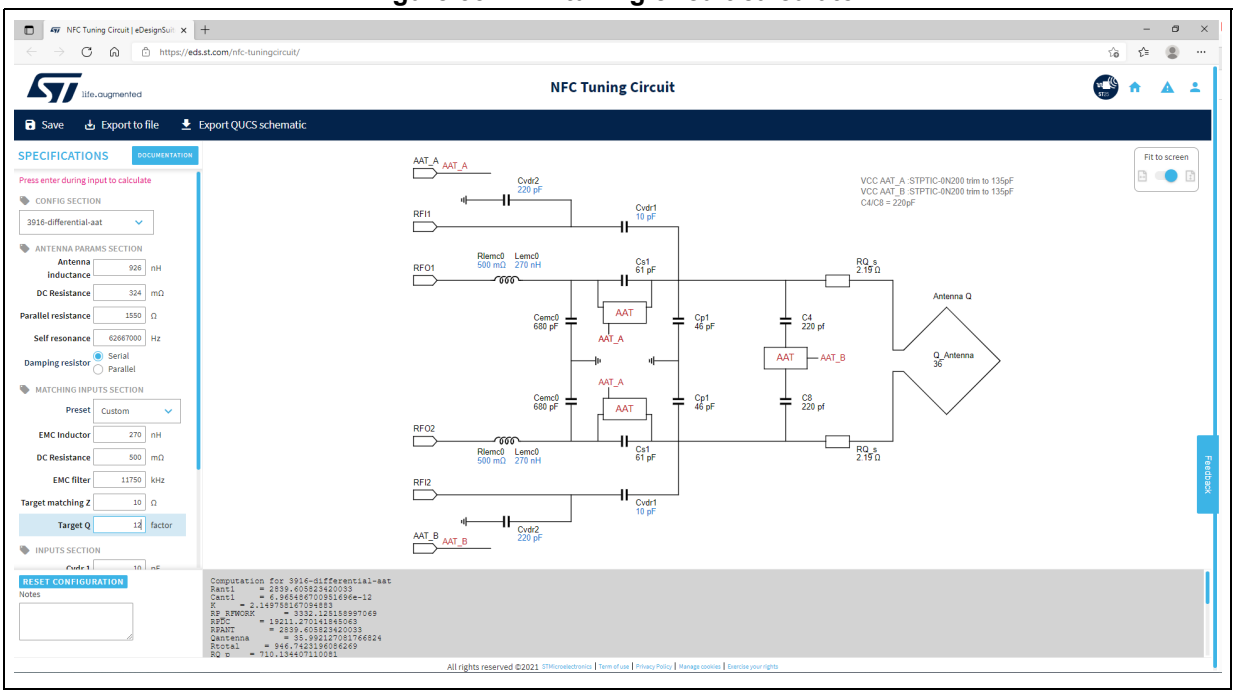
To compute the components value of the matching network located between the NFC reader and the antenna simply enter the antenna electrical parameters and matching targets values, and select the topology of the matching network.

The tool returns the complete set of component values (including the capacitors in the AAT circuit) requested to achieve the desired design targets.

The circuit can then be exported as a Qucs file to further analyze and optimize the design.

An on-line version of the tool is available at https://eds.st.com.

Figure 33. NFC tuning circuit calculator



8 Conclusion

This document describes the basic antenna design and tuning process for the ST25R3916, ST25R3917 and ST25R3920 devices.

It helps the user to define the output power of the reader, specifying the components like EMC inductors used for the matching network. It also guides through the measurements of the antenna parameters, and the computation and simulation of the matching network.

The last section is dedicated to basic design verification steps, to ensure that the matching network is properly defined.

9 Revision history

Table 3. Document revision history

Date	Revision	Changes
25-Jan-2019	1	Initial release.
26-Feb-2019	2	Document classification changed from ST restricted to Public.
24-Aug-2020	3	Document scope extended to ST25R3917 and ST25R3920 devices. Updated document title and *Introduction*. Minor text edits across the whole document.
19-Jul-2021	4	Updated *Figure 19: ST25R antenna matching tool - Main window*, *Figure 20: ST25R antenna matching tool - Calculated matching components*, *Figure 21: Simulation parameters*, *Figure 22: S-parameter model*, *Figure 23: Transient simulation*, *Figure 24: AC simulation*, *Figure 25: Simulation results of the S-parameter and the AC model*, *Figure 26: Simulation results of the transient and of the AC model* and *Figure 32: Target matching impedance measured with network analyzer*. Updated *Section 6.2.2: Results*. Added *Section 7.5: NFC tuning circuit calculation*. Minor text edits across the whole document.
04-May-2022	5	Document scope extended to ST25R3916B, ST25R3917B, ST25R3918, and ST25R3920B devices. Updated document title and *Introduction*. Minor text edits across the whole document.