


FPGA Configuration PROM Parallel/Serial 4M-bit 2.5V/3.3V 44-Pin VQFP

Manufacturer:	AMD Xilinx, Inc
Package/Case:	QFP
Product Type:	Programmable Logic ICs
RoHS:	RoHS Compliant/Lead free 
Lifecycle:	Obsolete



Images are for reference only

[Inquiry](#)

General Description

Xilinx introduces the XC18V00 series of in-system programmable configuration PROMs (Figure 1). Devices in this 3.3V family include a 4-megabit, a 2-megabit, a 1-megabit, and a 512-kilobit PROM that provide an easy-to-use, cost-effective method for reprogramming and storing Xilinx FPGA configuration bitstreams.

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. A short access time after CE and OE are enabled, data is available on the PROM DATA (D0) pin that is connected to the FPGA DIN pin. New data is available a short access time after each rising clock edge. The FPGA generates the appropriate number of clock pulses to complete the configuration. When the FPGA is in Slave Serial mode, the PROM and the FPGA are clocked by an external clock.

When the FPGA is in Master SelectMAP mode, the FPGA generates a configuration clock that drives the PROM. When the FPGA is in Slave Parallel or Slave SelectMAP mode, an external oscillator generates the configuration clock that drives the PROM and the FPGA. After CE and OE are enabled, data is available on the PROM's DATA (D0-D7) pins. New data is available a short access time after each rising clock edge. The data is clocked into the FPGA on the following rising edge of the CCLK. A free-running oscillator can be used in the Slave Parallel or Slave SelectMAP modes.

Multiple devices can be cascaded by using the CEO output to drive the CE input of the following device. The clock inputs and the DATA outputs of all PROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family or with the XC17V00 one-time programmable serial PROM family.

Key Features

In-System Programmable 3.3V PROMs for Configuration of Xilinx FPGAs
Endurance of 20,000 Program/Erase Cycles

Program/Erase Over Full Industrial Voltage and Temperature Range (–40°C to +85°C)

IEEE Std 1149.1 Boundary-Scan (JTAG) Support

JTAG Command Initiation of Standard FPGA Configuration

Simple Interface to the FPGA

Cascadable for Storing Longer or Multiple Bitstreams

Low-Power Advanced CMOS FLASH Process

Dual Configuration Modes
Serial Slow/Fast Configuration (up to 33 MHz)

Parallel (up to 264 Mb/s at 33 MHz)

5V-Tolerant I/O Pins Accept 5V, 3.3V and 2.5V Signals

3.3V or 2.5V Output Capability

Design Support Using the Xilinx ISE™ Foundation™ Software Packages

Available in PC20, SO20, PC44, and VQ44 Packages

Lead-Free (Pb-Free) Packaging

Recommended For You

XC128XFT64C

AMD Xilinx, Inc

BGA

XC18V04VQ44I

AMD Xilinx, Inc

QFP

XC17128EPD8I

AMD Xilinx, Inc

DIP8

XC1765ELSO8C

AMD Xilinx, Inc

SOP8

XC18V04VQ44C

AMD Xilinx, Inc

QFP44

XC18V01SO20C

AMD Xilinx, Inc

SOP20

XCf32PVOG48C

AMD Xilinx, Inc

TSOP48

XC18V01PCG20C

AMD Xilinx, Inc

PLCC20

XCf04SVO20C

AMD Xilinx, Inc

TSSOP20

XC2C256-7CPG132I

AMD Xilinx, Inc

BGA132

XCf04SVOG20C

AMD Xilinx, Inc

TSSOP20

XCf08PFS48C

AMD Xilinx, Inc

BGA

XC18V01VQ44C

AMD Xilinx, Inc

TQFP44

XC1765EPD8C

AMD Xilinx, Inc

DIP8

XC18V02VQG44C

AMD Xilinx, Inc

QFP44