UM11111

PCAL6416AEV test board user manual

Rev. 1.0 — 12 April 2018 User manual

Document information

Information	Content
Keywords	PCAL6416AEV, OM13260, OM13320, OM13303
Abstract	This user manual describes how to use NXP's PCAL6416AEV test board.

Revision history

Rev	Date	Description
v.1	20180412	Initial version

1 Introduction

This user manual describes how to use NXP's PCAL6416AEV test board. This board is designed for testing functional characteristics of the PCAL6416AEV part, saving time for NXP customer qualification of the 16-bit Agile GPIO expander. This board works with NXP's Fm+ demo board (OM13260) or any customer I^2C-bus controller. It has a socket for VFPGA24 3x3 mm, a 14-pin connector for FM+ demo board using 3.3V, and two external power supply TPs for VDDI and VDDP of the PCAL6416AEV, as well as an I^2C-bus header for customer I^2C controller.

2 Features and benefits

- Direct connection to OM13320 Fm+ Development kit
- External I^2C-bus connection
- Isolated power rail for power measurement
- Socket of VFPGA24 3x3 mm with 0.30 mm ball size
- Flexible power supply configuration: 3.3V or external supply
- Direct connection to OM13303 GPIO Target board for I/O visualization
- Jumper configuration of device I^2C address
- LED indicators for power and INT
- Scope ground connection loop

3 Hardware description

1. Socket U1 for VFBGA24 3x3 mm with 0.30 mm ball size packet
2. Connection to Fm+ demo board (OM13260) port A, B, C or D: CN2 is a 2x8 female connector
3. Slave device address selection: J6 is a 2x2 male header
   a. Slave device address = 0x010-0001(42h) when 1-2 is connected
   b. Slave device address = 0x010-0000(40h) when 3-4 is connected
4. VDDI power selection: J4 is a 1x3 header. This jumper header is for selection VDDI (I2C and internal logic power). The power is from Fm+ demo board 3.3V or external power from TP3
   a. VDDI = TP3 (VDDI_IN: external power) when J4 is opened and J5 is connected
   b. VDDI = 3.3V from Fm+ demo board when J4: 1-2 is connected and J5 is connected
   c. VDDI = 5V from Fm+ demo board when J8: 1-2 & J4: 2-3 are connected and J5 is connected
5. VDDP (IO port) power selection: J1 is a 1x3 header. This jumper header is for selection VDDP (IO port power). The power is from Fm+ demo board 3.3V or external power form TP2.
   a. VDDP = TP2 (VDDP_IN: external power) when J1 is opened and J3 is connected
   b. VDDP = 3.3V from Fm+ demo board when J1: 2-3 is connected and J3 is connected
   c. VDDP = 5V from Fm+ demo board when J8: 1-2 & J1: 1-2 is connected and J3 is connected
6. VDDI external power input by TP3 (VDDI_IN) and TP4 (GND)
7. VDDP external power input by TP2 (VDDP_IN) and TP5 (GND)
8. External I2C SDA signal input from CN1 (SDA: Beagle master)

9. External I2C SCL signal input from CN2 (SCL: Beagle master)
10. CN3 and CN4 are 2x5 female headers connected to OM13303 GPIO Target board for I/O visualization
11. LED power for INT(D1) signal and VPP(D2) power indicator
12. J2 is Reset jumper for PCAL6416AEV

4 Using NXP PCAL6416AEV with Fm+ demo board

1. Get I2C Fm+ Development Board Kit package at: http://www.nxp.com/demoboard/OM13320.html
2. Connect CN2 of NXP PCAL6416AEV to any port A, B, C or D on Fm+ demo board
3. Set jumpers:
   - J1 = 2-3 for +3V3 for VDDP_IN
   - J3 = enabling power for VDDP
   - J4 = 1-2 for +3V3 for VDDI_IN
   - J5 = enabling power for VDDI
   - J6 = 3-4 for PCAL6416AEV slave address = 0x010-0000 (40h)
4. Set jumpers:
   - Use multi-meter at J3 for VDDP and J5 for VDDI
5. Test GPIO outputs and Interrupt
   a. Put jumper on J4:1-2 & J5 to enable power of D1 LED indicators for INT and PWR
   b. Connect OM13303GPIO Target Boards (Fm+ demo board kit) to CN3 and CN4
   c. Connect USB from Fm+ demo board to the PC with NXP Fm+ software

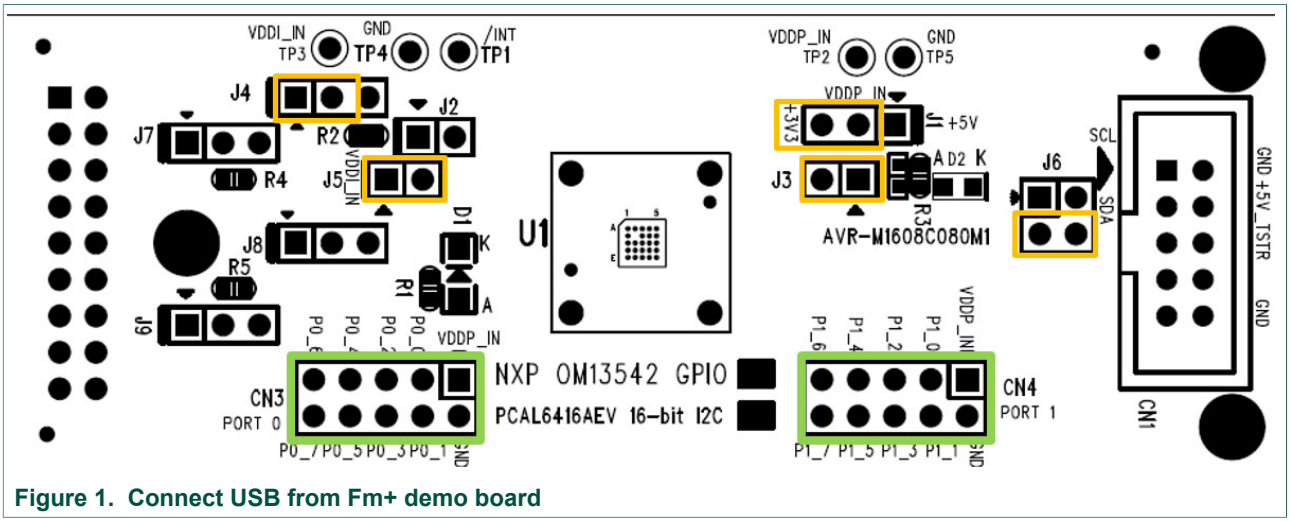

Figure 1. Connect USB from Fm+ demo board

6. Use NXP Fm+ GUI software:
   a. Open NXP Fm+ software

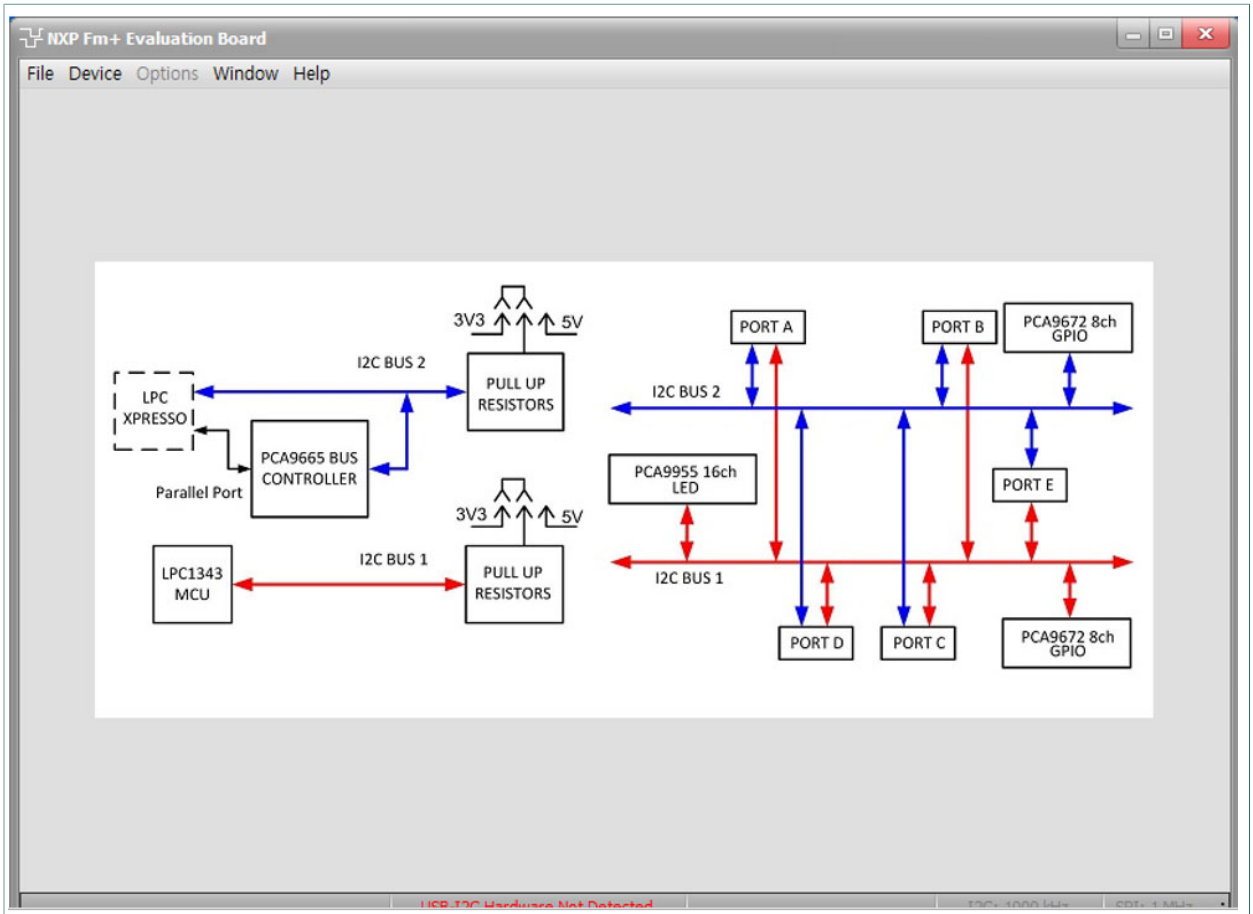

Figure 2. Open NXP Fm+

b. Go to Device Selection > I/O Expanders > 16-bit I/O Expanders > PCAL6416A

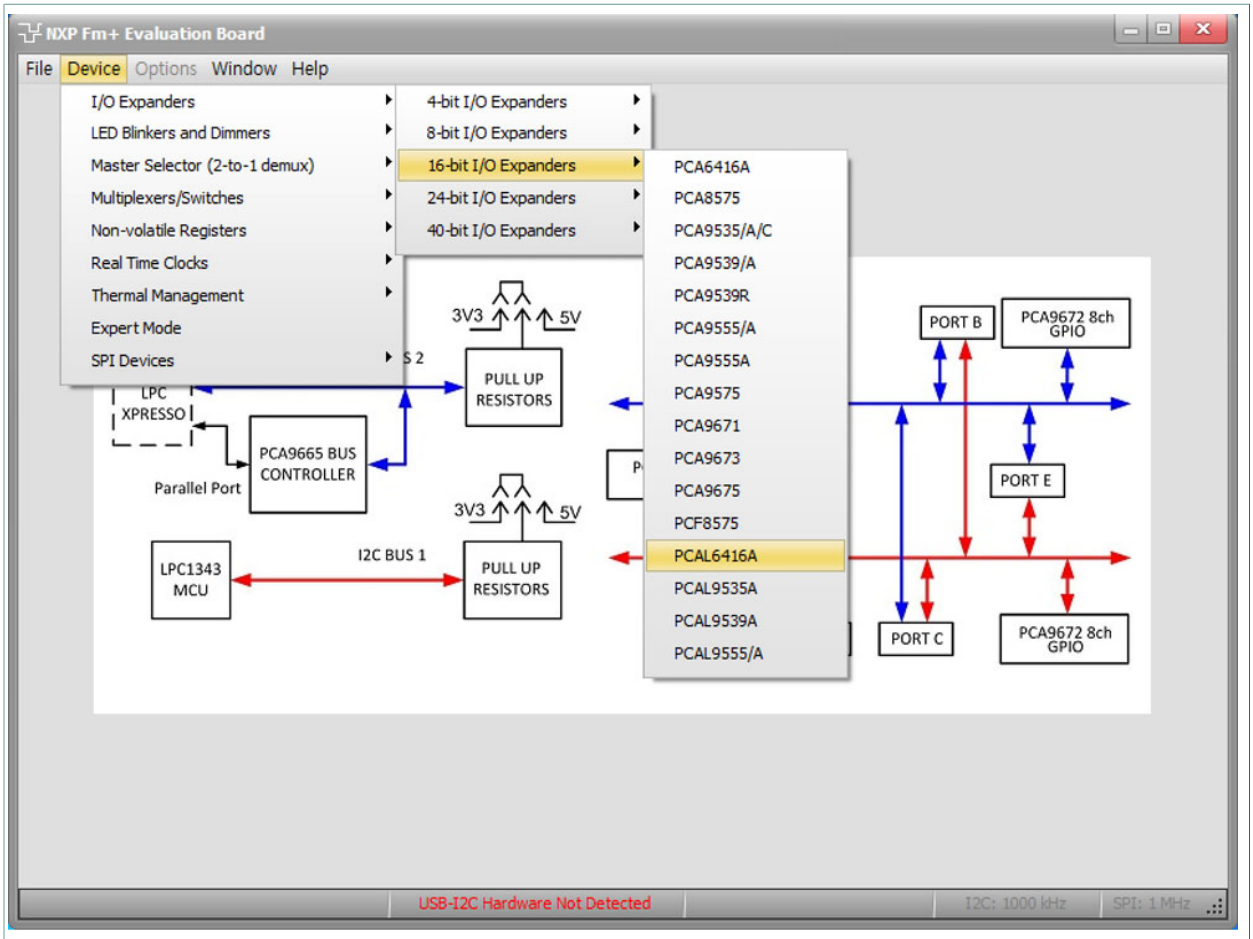

Figure 3. Go to device selection

c. Change Slave Address to 0x40 and make sure the Slave presence light is on

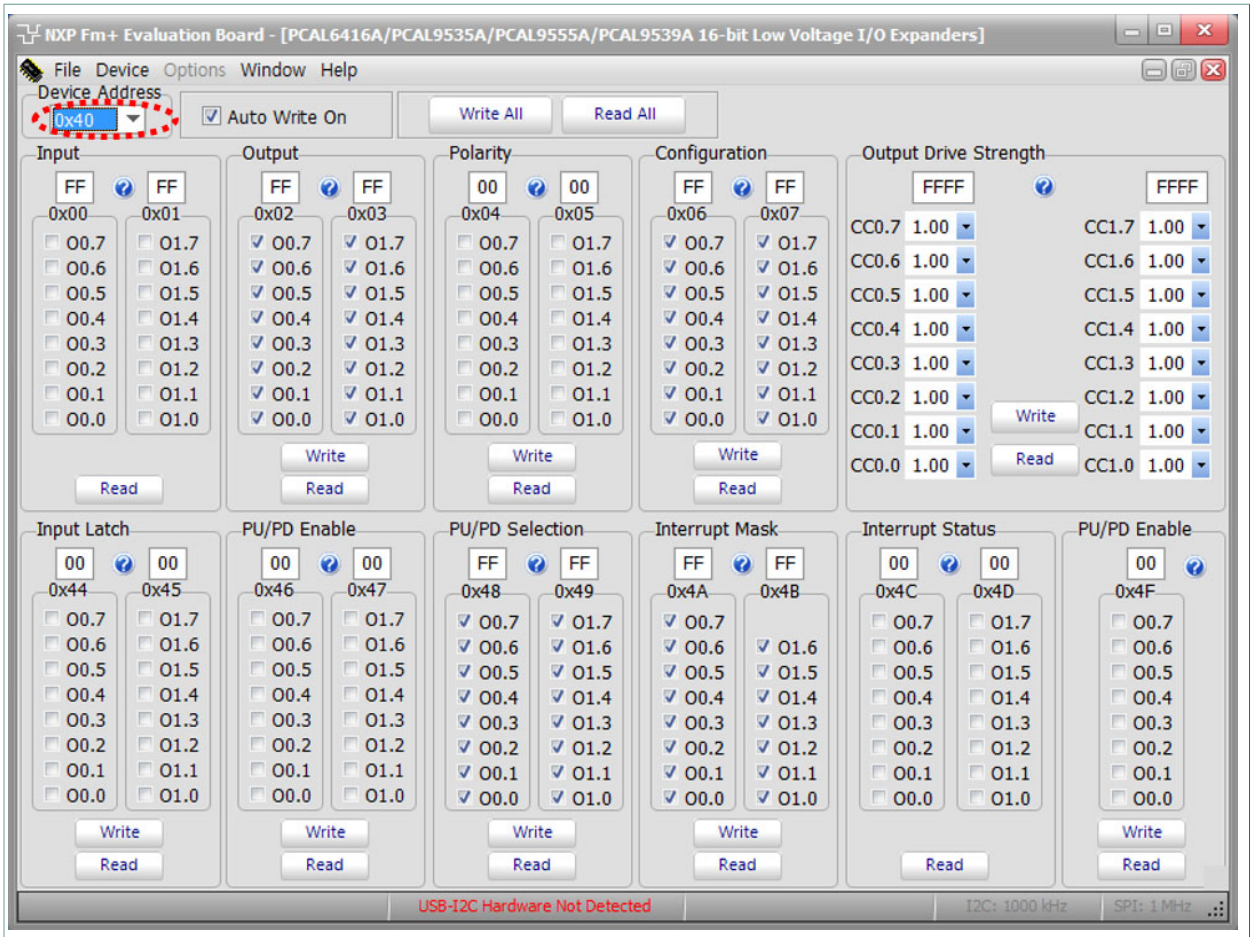

Figure 4. Change slave address to 0x40

d. The I/Os can be configured at input or output, input polarity changed, and output set high or low.

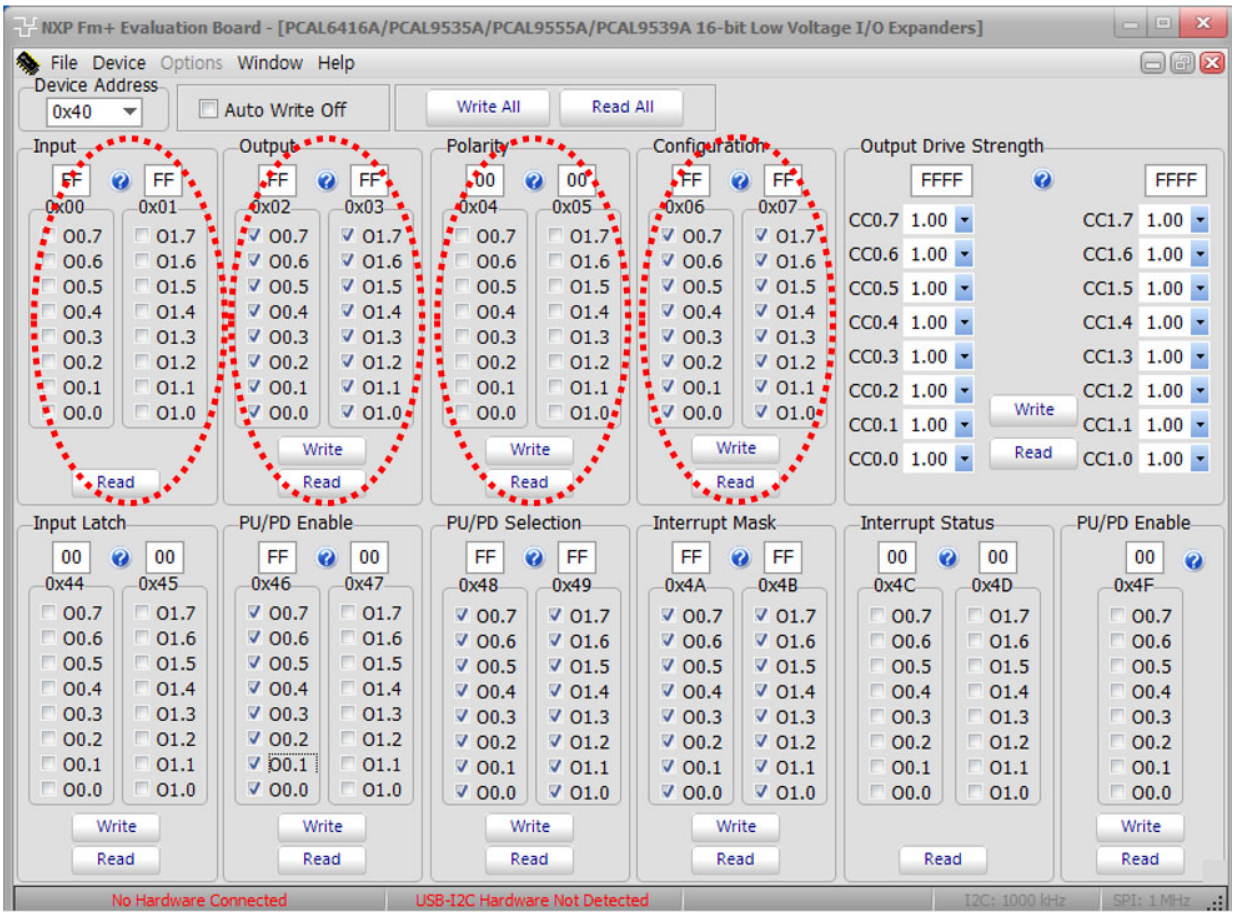

Figure 5. Configure I/Os

I/O interrupt status, interrupt mask enable/disable and input latch enable/disable.

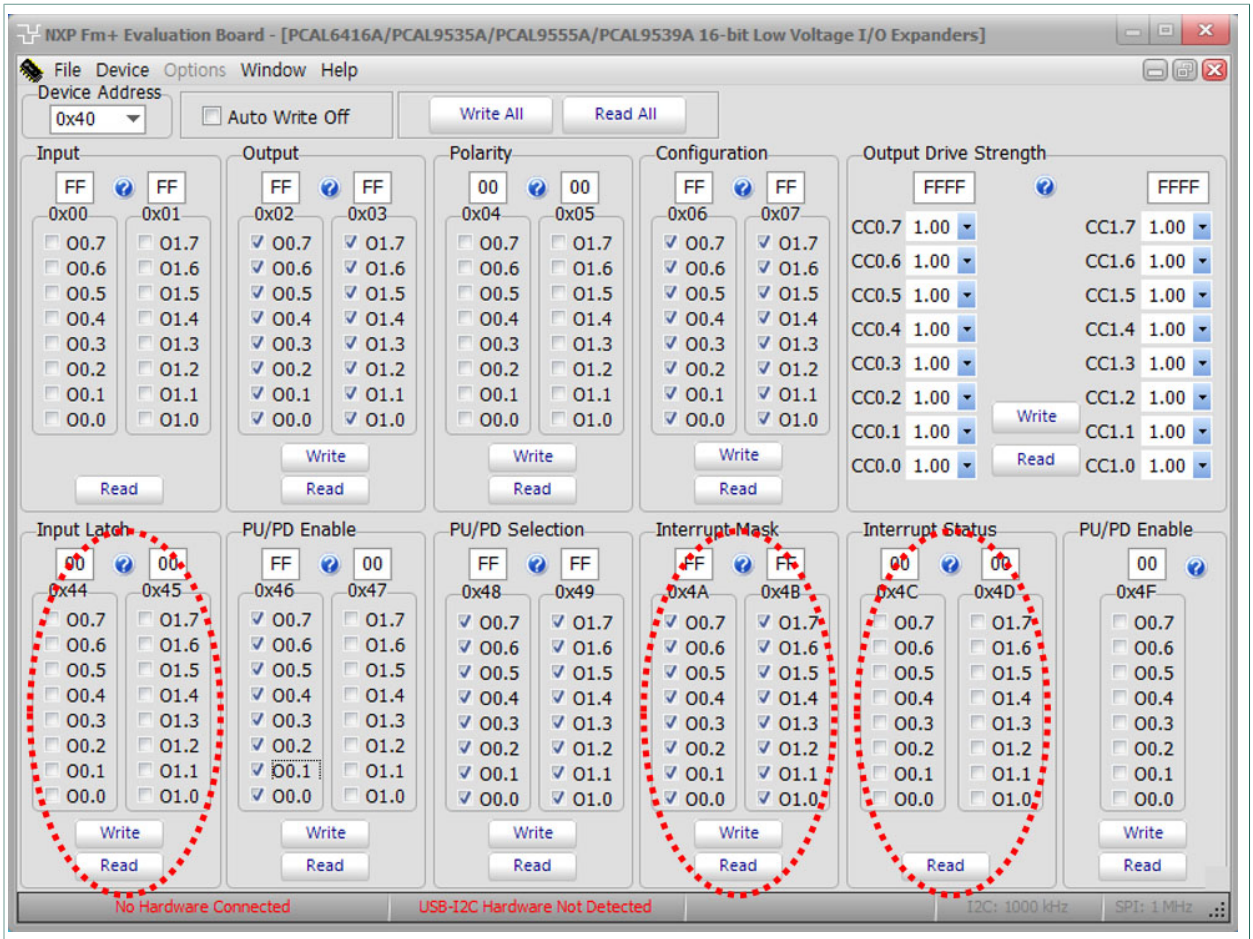

Figure 6. I/O interrupt status

If the port is set at output then that output port can change the drive strength.

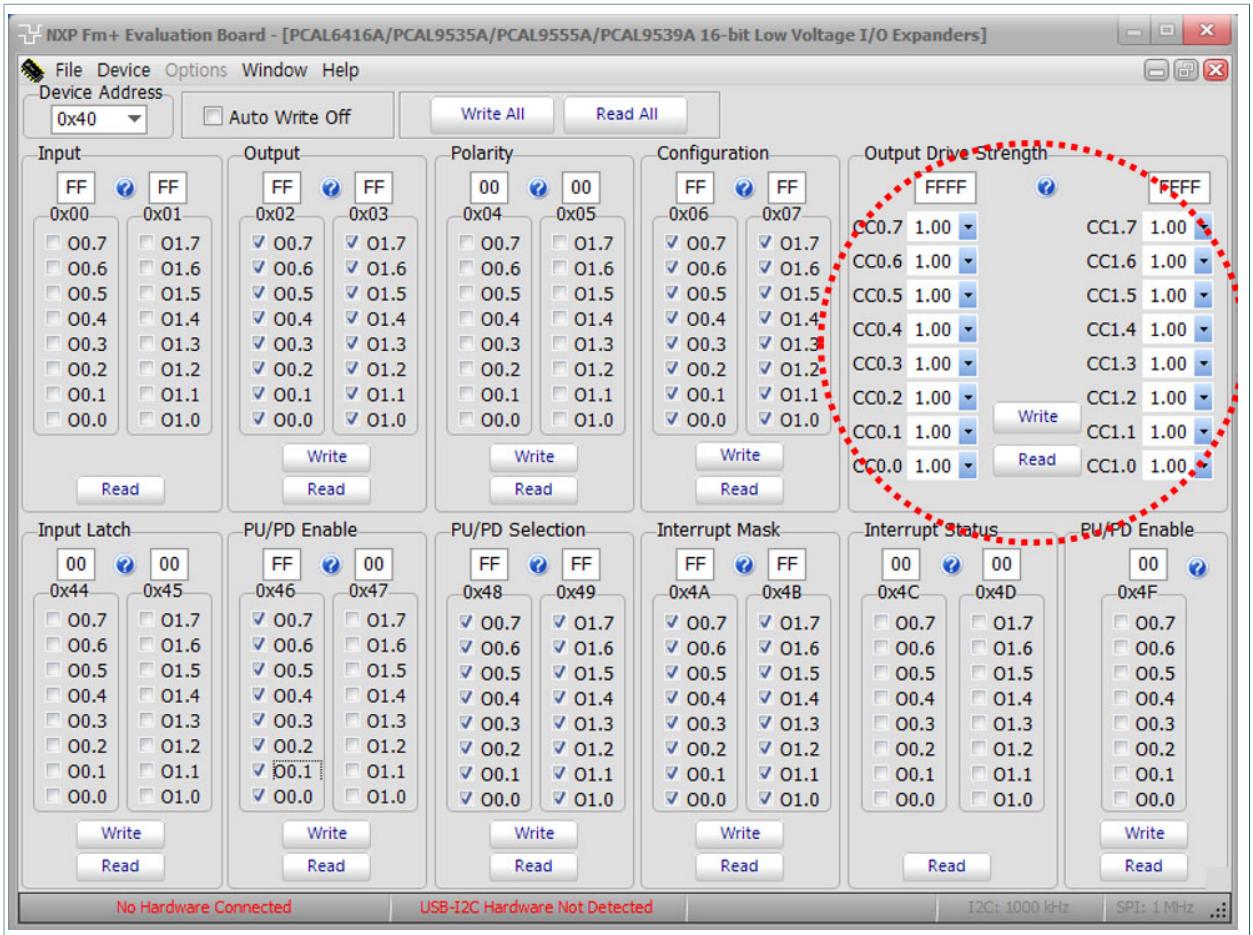

Figure 7. Output port

5 Using NXP PCAL6416AEV with customer system

1. Connect input power for VDDI and VDDP
   a. VDDI power is for I^2C-bus and internal logic of PCAL6416AEV. VDDI can be input from external power by TP3.
   b. VDDP power is for I/O ports of PCAL6416AEV. VDDP can be input from external power by TP2.
2. Set jumpers:
   - J1 = open for external power for VDDP_IN
   - J3 = enable power for VDDP
   - J4 = open for external power for VDDI_IN
   - J5 = enable power for VDDI
   - J6 = 3-4 for PCAL6416AEV slave address = 0x010-0000
   - TP2 = external power 3.3V for VDDP_IN with TP5 (GND)
   - TP3 = external power 3.3V for VDDI_IN with TP4 (GND)
3. Test current of VDDI and VDDP
   - Use multi-meter at J3 for VDDP and J5 for VDDI.
4. Test GPIO outputs and Interrupt
   a. Put jumper on J4 to enable power of D1 LED indicators for INT and PWR

b. Connect OM13303 GPIO Target Boards to CN3 and CN4
c. Output Low to make the LED light turn on, output high to make LED light turn off

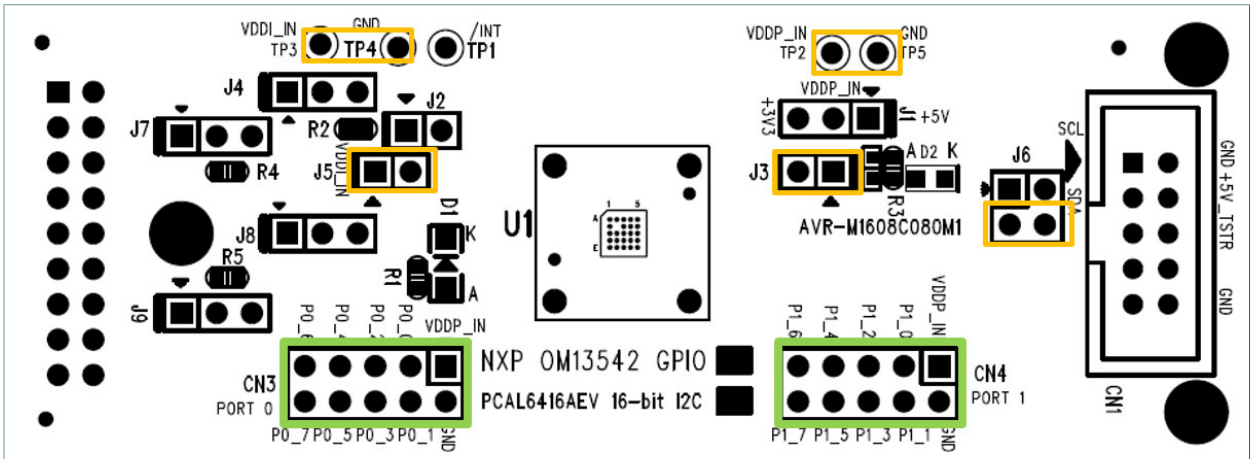

Figure 8. Test GPIO outputs and interrupt

6 Layout

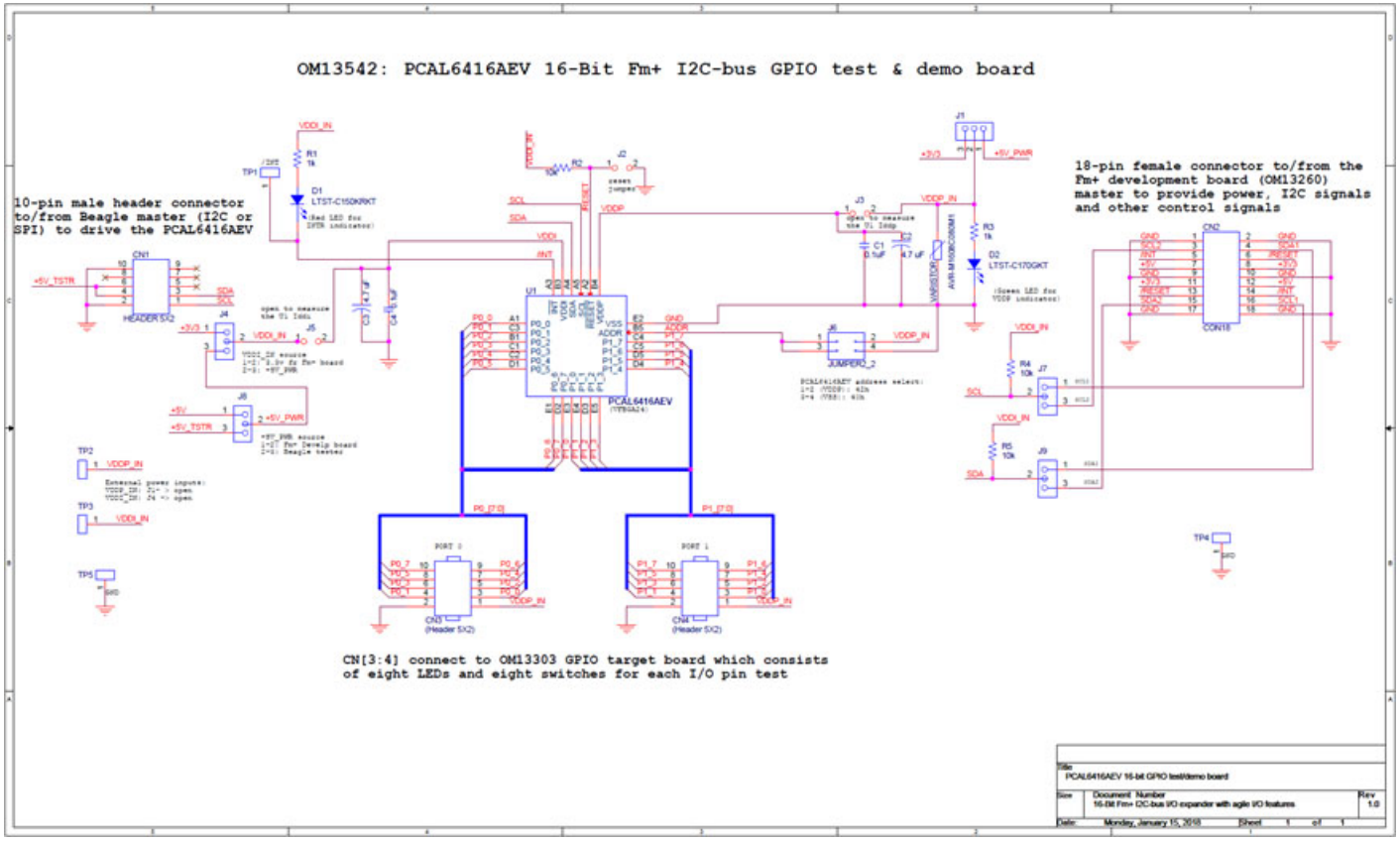

Figure 9.

7 Notes

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Figures

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