Application Report

TPS61378-Q1, TPS613781-Q1, TPS613782-Q1, TPS613783-Q1, TPS613784-Q1, and TPS613785-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

1 Overview

This document contains information for TPS61378-Q1, TPS613781-Q1, TPS613782-Q1, TPS613783-Q1, TPS613784-Q1, TPS613785-Q1(VQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

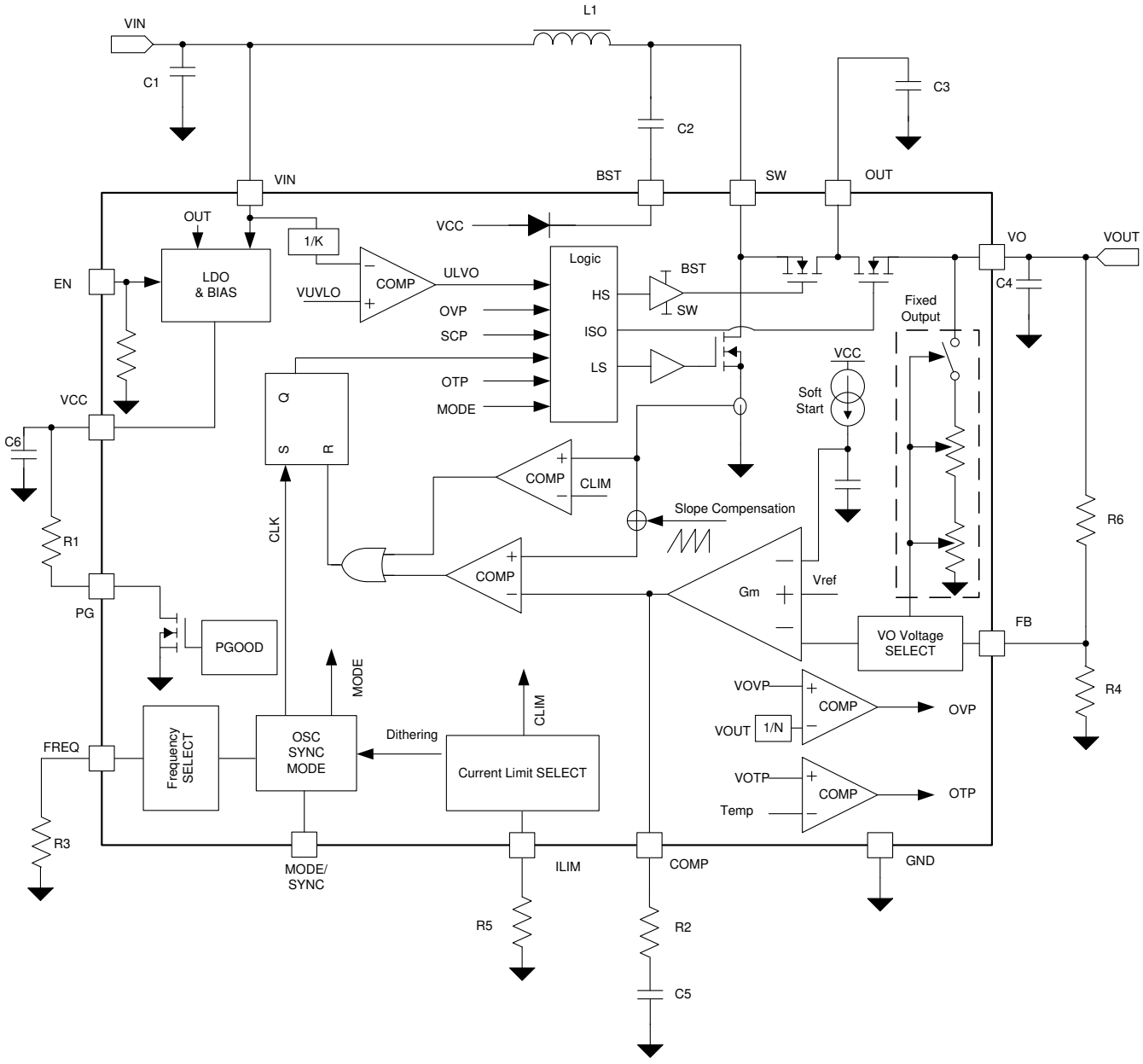

Figure 1-1. Functional Block Diagram

TPS61378-Q1, TPS613781-Q1, TPS613782-Q1, TPS613783-Q1, TPS613784-Q1, TPS613785-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS61378-Q1, TPS613781-Q1, TPS613782-Q1, TPS613783-Q1, TPS613784-Q1, TPS613785-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	14
Die FIT Rate	7
Package FIT Rate	7

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 750 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs Analog & Mixed =<50V supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS61378-Q1, TPS613781-Q1, TPS613782-Q1, TPS613783-Q1, TPS613784-Q1, TPS613785-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VO No output GND or HIZ	50%
VO output not in specification voltage or timing	40%
Load disconnect stuck on	5%
PG false trip, fails to trip	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS61378-Q1, TPS613781-Q1, TPS613782-Q1, TPS613783-Q1, TPS613784-Q1, TPS613785-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS61378-Q1, TPS613781-Q1, TPS613782-Q1, TPS613783-Q1, TPS613784-Q1, TPS613785-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the TPS61378-Q1 datasheet.

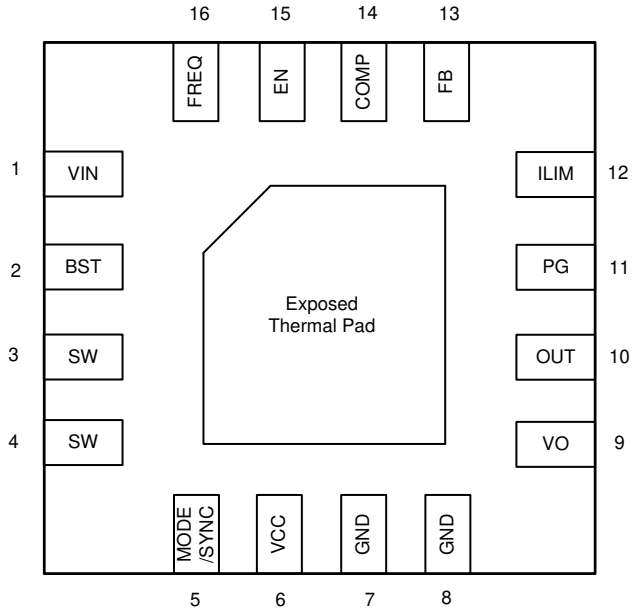

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the 'Recommended Operating Conditions' and the 'Absolute Maximum Ratings' found in the TPS61378-Q1 data sheet.
- Configuration as shown in the 'Application and Implementation' found in the TPS61378-Q1 data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects(s)	Failure Effect Class
VIN	1	Device will not operate. Power supply is short.	B
BST	2	Possibe device damage.	A

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects(s)	Failure Effect Class
SW	3	Potential damage to inductor and pin.	A
SW	4	Potential damage to inductor and pin.	A
MODE/SYNC	5	For TPS61378-Q1, TPS613781-Q1, TPS613782-Q1, device will remain in auto PFM mode. Loss of forced PWM mode, spread spectrum functionality and frequency synchronization functionality.	C
		For TPS613783-Q1, TPS613784-Q1, TPS613785-Q1, device will remain in auto PFM mode. Loss of forced PWM mode and frequency synchronization funtionality.	
VCC	6	Output voltage out of regulation.	B
GND	7	No effect.	D
GND	8	No effect.	D
VO	9	Device will reamin in hiccup output short circuit protection mode.	B
OUT	10	Potential damage to device.	A
PG	11	Correct output voltage. Loss of PG functionality.	C
ILIM	12	Correct output voltage. Peak switch current limit is maximum and can't be configured.	C
FB	13	For TPS61378-Q1, TPS613783-Q1, Vout = 5 V.	B
		For TPS613781-Q1, TPS613784-Q1, Vout = 5.7 V.	
		For TPS613782-Q1, TPS613785-Q1, Vout = 9 V.	
COMP	14	No output voltage.	B
EN	15	Loss of ENABLE functionality. Device will remain in shut-down mode.	B
FREQ	16	Switching frequency is 2MHz typically.	C

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects(s)	Failure Effect Class
VIN	1	Device doesn’t work. Vout = 0 V.	B
BST	2	Device damaged.	A
SW	3	Possible device damage.	A
SW	4	Possible device damage.	A
MODE/SYNC	5	For TPS61378-Q1, TPS613781-Q1, TPS613782-Q1, device will remain in auto PFM mode. Loss of forced PWM mode, spread spectrum functionality and frequency synchronization functionality.	C
		For TPS613783-Q1, TPS613784-Q1, TPS613785-Q1, device will remain in auto PFM mode. Loss of forced PWM mode and frequency synchronization functionality.	
VCC	6	High ripple on VCC pin. Effeiciency is lower.	C
GND	7	Possible device damage.	A
GND	8	Possible device damage.	A
VO	9	No output voltage.	B
OUT	10	Possible device damage.	A
PG	11	Correct output voltage. Loss of PG functionality.	C
ILIM	12	Output current capability decreases.	B
FB	13	Output voltage is out of regulation.	B
COMP	14	Output voltage is out of regulation.	B
EN	15	Loss of ENABLE functionality. Device will remain in shut-down mode.	B
FREQ	16	No output voltage.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects(s)	Failure Effect Class
VIN	1	BST	Possible device damage.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects(s)	Failure Effect Class
BST	2	SW	Output voltage out of regulation.	B
SW	3	SW	No effect.	D
SW	4	MODE/SYNC	Possible device damage.	A
MODE/SYNC	5	VCC	Device will remain in forced PWM mode. Loss of auto PFM mode and frequency synchronization functionality.	C
VCC	6	GND	Device doesn't work. Vout = 0 V.	B
GND	7	GND	No effect.	D
GND	8	VO	Device will reamin in hiccup output short circuit protection mode.	B
VO	9	OUT	Loss of down mode functionality and hiccup output short circuit protection.	B
OUT	10	PG	Possible device damage.	A
PG	11	ILIM	Potential device damage if PG is pulled up to higher than 6 V.	A
ILIM	12	FB	OVP is triggered.	B
FB	13	COMP	No output voltage.	B
COMP	14	EN	OVP is triggered.	B
EN	15	FREQ	No output voltage.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects(s)	Failure Effect Class
VIN	1	No effect.	D
BST	2	Possible device damage.	A
SW	3	Damage to internal power FETs.	A
SW	4	Damage to internal power FETs.	A
MODE/SYNC	5	MODE/SYNC pin damaged if supply voltage is higher than 6 V.	A
VCC	6	VCC pin damaged if supply voltage is higher than 6 V.	A
GND	7	Possible device damage due to large current.	A
GND	8	Possible device damage due to large current.	A
VO	9	Vo = Vin.	B
OUT	10	Device ramain in hiccup mode. No output voltage.	B
PG	11	Possible device damage.	A
ILIM	12	ILIM pin damaged if supply voltage is higher than 6 V.	A
FB	13	FB pin damaged if supply voltage is higher than 6 V.	A
COMP	14	COMP pin damaged if supply voltage is higher than 6 V.	A
EN	15	EN pin damaged if supply voltage is higher than 6 V.	A
FREQ	16	FREQ pin damaged if supply voltage is higher than 6 V.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2020) to Revision C (October 2020) **Page**

- Added TPS613781-Q1, TPS613782-Q1, TPS613783-Q1, TPS613784-Q1, TPS613785-Q1 2
- Changed functional block diagram 2

Changes from Revision A (June 2020) to Revision B (August 2020) **Page**

- Added Pin FMA 5

Changes from Revision * (May 2020) to Revision A (June 2020)	Page
• Removed reference of Pin FMA	2

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