

Frequency Divider Operation and Compensation with No Input Signal

INTRODUCTION

The Analog Devices, Inc., prescaler product line includes more than 10 low noise, static dividers utilizing indium gallium phosphide (InGaP) and gallium arsenide (GaAs) heterojunction bipolar transistor (HBT) technology that accept a broad range of input signals, from dc (with a square wave input) through 18 GHz microwave frequencies. Division ratios of 2, 3, 4, 5, and 8 are available together with 3 V and 5 V single-supply versions. These divider products exhibit very low additive single-sideband (SSB) phase noise with the best products delivering -153 dBc/Hz at 100 kHz offset, enabling synthesizer designers to maintain excellent system noise performance. This application note describes how to prevent self oscillation and subsequent false triggers in the dividers when no radio frequency (RF) power is presented at the device input.

APPLICATION PROBLEM

Dividers are used in a wide variety of applications ranging from consumer electronics to military and satellite systems. Specifically, dividers are incorporated in circuits such as phase-locked loops (PLLs) or synthesizers. In each of these applications, the RF signal is continuously incident on the input of the frequency divider, presenting it with a constant dominant signal (signal-to-noise ratio (SNR) high). However, other applications may

not present a continuous RF signal to the input, thereby leaving the input vulnerable to noise (SNR low). One such application is a signal detection circuit, shown in Figure 1. This circuit detects the presence of RF energy by directly downconverting through multiple divider circuits and performing an analog-to-digital transformation. The signal detection circuitry determines the frequency and then outputs the appropriate response.

When no input is present, the inputs to the dividers are subjected to noise. Because the dividers are designed for maximum sensitivity, the input stages have a tendency to self oscillate with no or low signal input levels. This self oscillation tendency also causes the dividers to malfunction when the input signal slew rate is too low, such as with low frequency sine waves. Because the divider network is essentially digital in nature, any signal with a sufficient level triggers a gate within the divider; the divider produces an output due to this false trigger. This output appears as multiple tones when viewed on a spectrum analyzer. The tones are detected by the signal detection circuitry, causing a false output to occur. Therefore, it is essential to prevent the divider from false triggering in the absence of an RF signal. To prevent this condition, an offset voltage is applied across the inputs of the dividers to prevent the self oscillation and, therefore, the false triggering of the divider in the absence of a signal.

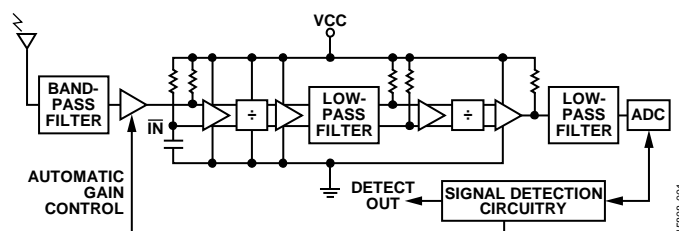


Figure 1. Signal Detection Circuit

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REVISION HISTORY

5/2017—v.00.1103 to Rev. A
Updated Format Universal
Changed HMC364S8G to HMC365S8G and
R to R5..... Throughout
Changed General Description Section to Introduction Section 1

Changes to Introduction Section1
Changes to Limitations and Trade-Offs Section, Figure 7
Caption, and Table 14

APPLICATION SOLUTION

A typical divider circuit consists of three main components: a differential amplifier at the input, one or more digital divider networks, and an output differential amplifier (see Figure 2). The input differential amplifier creates a digital like output that, depending on the voltage levels, triggers gates in the digital divider networks. The output differential amplifier receives the digital output and amplifies it accordingly.

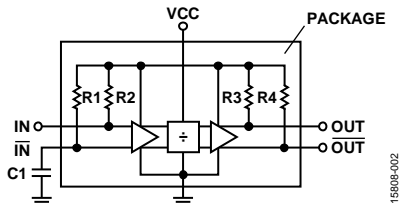


Figure 2. Block Diagram of Typical Frequency Divider

The input/output differential amplifiers have pull-up resistors, R1 to R4 (on chip), connected to VCC. Capacitor C1 is external and ties the complementary input to RF ground for single-ended input operation. Because the resistances of R1 and R2 are equal, the difference in potential across the input terminals is zero when no RF is present. When the amplifier is in this state, any noise present at the input is amplified and causes the digital divider to false trigger. However, when a nominal value of RF power is present at the input port, current draw through R2 creates a voltage drop across R2, resulting in a potential difference across the input terminals. In this state, the noise is suppressed and the false triggering prevented.

By placing a resistor from the complementary input port to ground, a potential difference is established across the input ports, thereby preventing false triggering of the divider when no RF is applied.

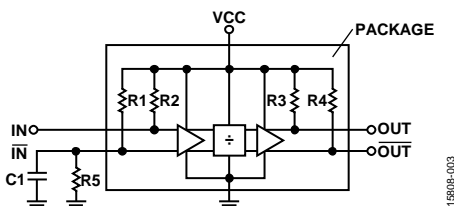


Figure 3. Block Diagram of Typical Frequency Divider with Offset Voltage Compensation

Figure 3 shows a schematic of a typical divider with Offset Resistor R5 placed at the complementary input port. The value of the resistance is initially chosen to allow approximately a 25 mV voltage differential between the input terminals but may be higher depending on the divider used. Place the resistor as physically close to the pin as possible to minimize parasitics.

Offset resistors were placed at the inputs of these dividers, evaluated over temperature (-40°C to $+85^{\circ}\text{C}$) with and without an RF signal applied. Figure 4 shows a typical evaluation board configured with an offset resistor, R5.

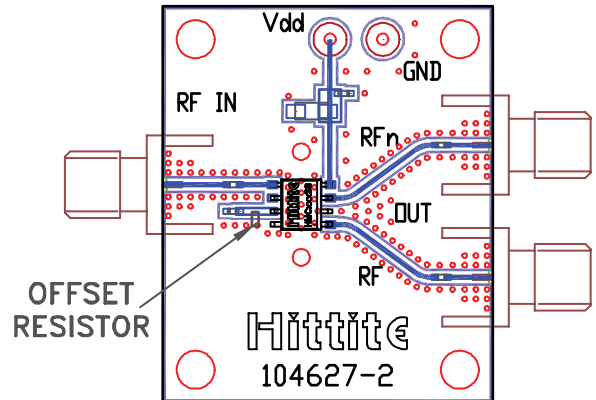


Figure 4. HMC362S8G Evaluation Board with Offset Resistance

Figure 5 and Figure 6 show plots of the spectrum, at the output of the HMC362S8G divider, from dc to 20 GHz. Figure 5 shows the output spectrum when no RF is applied and with no offset resistor at the complementary input. The multiple tone output is caused by the false triggering of the digital divider. Figure 6 shows the spectrum under the same conditions but with an offset resistor at the complementary input. The divider produces no output over the temperature range of -40°C to $+85^{\circ}\text{C}$.

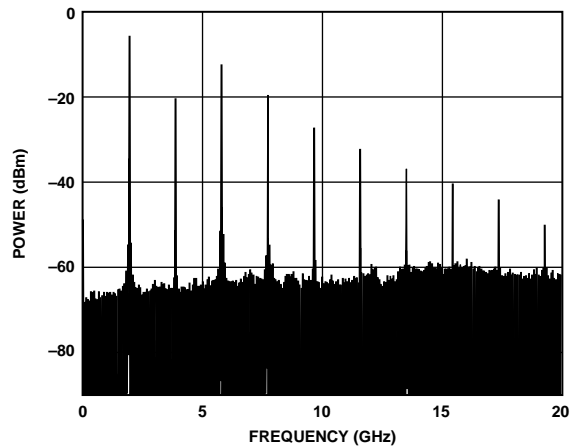


Figure 5. Divider Output with No Input and No Offset Resistance

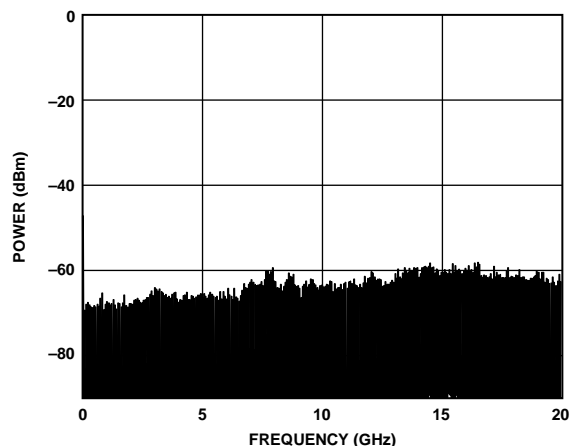


Figure 6. Divider Output with 40 kΩ Offset Resistance

The majority of Analog Devices dividers have differential inputs/outputs. However, three dividers are designed with single-ended inputs/outputs. The exceptions are the [HMC432](#), [HMC433](#), and [HMC434](#). Although these devices have single-ended inputs, they still require offset resistances because, internally, the inputs are differential but have been terminated for single-ended operation.

LIMITATIONS AND TRADE-OFFS

The input sensitivity of the divider is affected by the offset voltage created by the offset resistor. Figure 7 shows the input sensitivity of the [HMC362S8G](#) with and without the offset resistor. The solid lines outline the upper and lower range of the input sensitivity of the divider with no offset resistor.

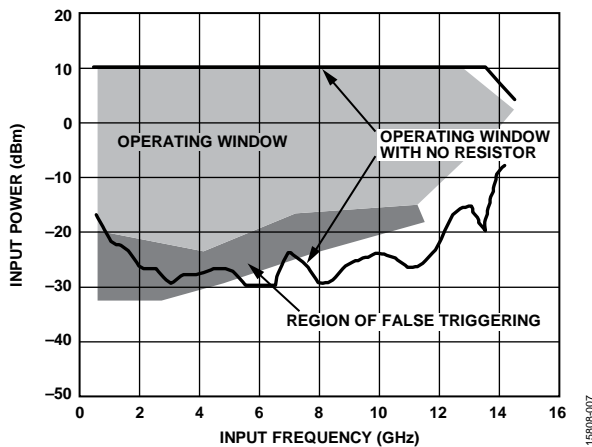


Figure 7. [HMC362S8G](#) Input Sensitivity With and Without Offset Resistor

When using an offset resistor, the minimum input power required for proper operation is higher, as outlined by the lower boundary of the light gray shaded area. The upper boundary of the light gray shaded area is the maximum allowable input power.

For the divider to produce output, RF power must be applied at the input. Without RF power, the divider produces no output; however, there is still a region where the divider can produce a false trigger. This area is marked by the dark gray shaded area. In this region, the voltage differential across the input goes to zero (or close to it) due to the increased input signal. With increasing input power, the voltage differential across the input is reestablished and the divider operates normally.

CONCLUSION

Analog Devices dividers provide exceptional reliability and performance in a variety of systems. In the majority of systems, these dividers require no special biasing. However, there are systems in which the dividers may false trigger, which normally occurs in systems where the input of the divider experiences periods of no RF power present at the input. During these periods, the divider may produce false triggers due to noise present at the input. To prevent these false triggers, apply an offset voltage across the input. This offset voltage is created by simply placing a shunt resistor from the complementary input to ground.

Table 1 shows the recommended values of offset resistors for these dividers over the temperature range of -40°C to $+85^{\circ}\text{C}$. The input power sensitivity plots for these dividers, with and without offset resistors, are shown in Figure 8 to Figure 16.

Table 1. Offset Resistances for Analog Devices Dividers

| Divider Product No. | Offset Resistance, R5 (kΩ) | Comments |
|---------------------------|----------------------------|--------------------------------------|
| HMC361S8G | 40 | Offset resistor from Pin 7 to ground |
| HMC362S8G | 40 | Offset resistor from Pin 7 to ground |
| HMC363S8G | 60 | Offset resistor from Pin 7 to ground |
| HMC365S8G | 60 | Offset resistor from Pin 7 to ground |
| HMC432 | 4 | Offset resistor from Pin 3 to ground |
| HMC433 | 4 | Offset resistor from Pin 3 to ground |
| HMC434 | 4 | Offset resistor from Pin 3 to ground |
| HMC437 | None | No resistor required |
| HMC438 | None | No resistor required |

Input Power Sensitivity Plots

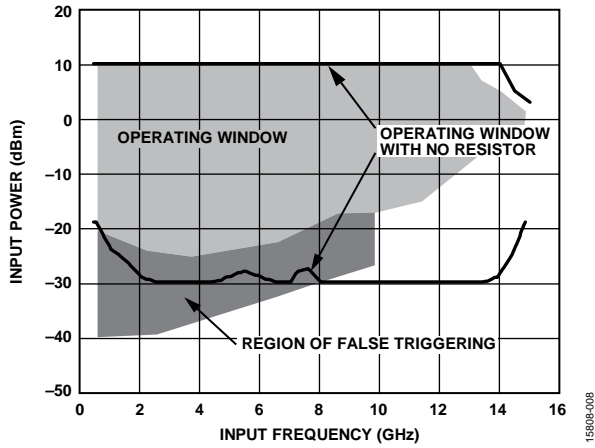


Figure 8. HMC361S8G Input Sensitivity and Operation, $R_5 = 40 \text{ k}\Omega$

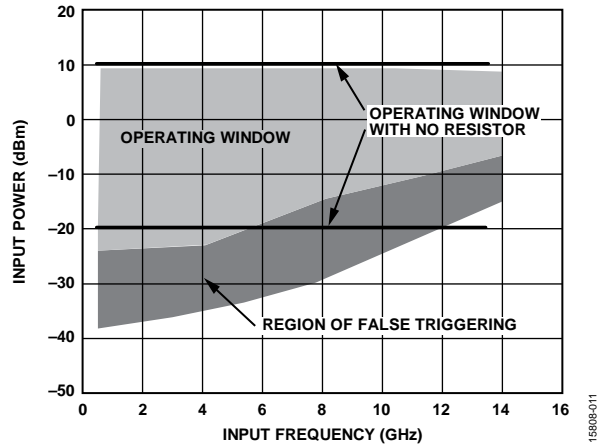


Figure 11. HMC365S8G Input Sensitivity and Operation, $R_5 = 60 \text{ k}\Omega$

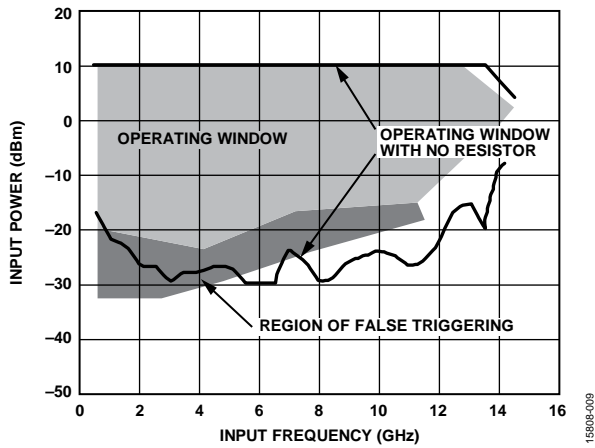


Figure 9. HMC362S8G Input Sensitivity and Operation, $R_5 = 40 \text{ k}\Omega$

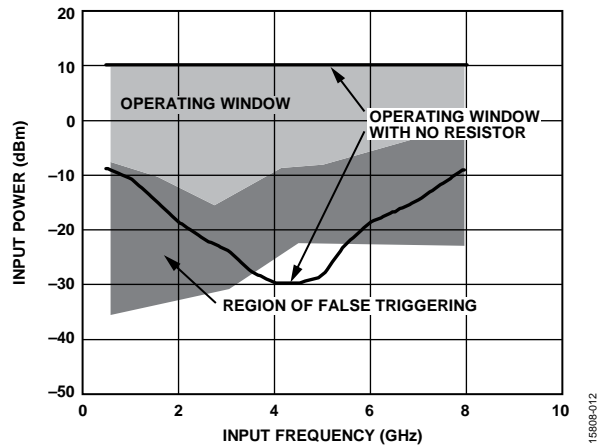


Figure 12. HMC432 Input Sensitivity and Operation, $R_5 = 4 \text{ k}\Omega$

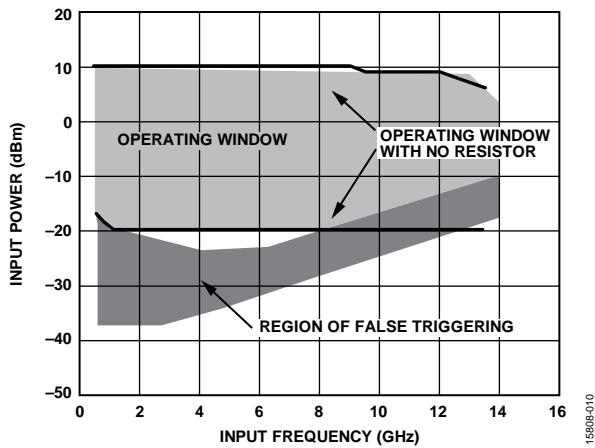


Figure 10. HMC363S8G Input Sensitivity and Operation, $R_5 = 60 \text{ k}\Omega$

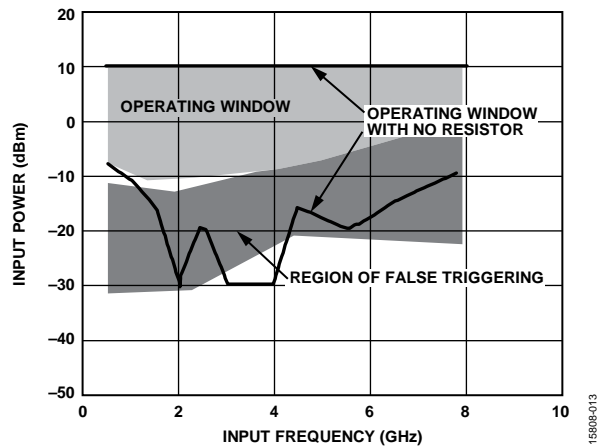


Figure 13. HMC433 Input Sensitivity and Operation, $R_5 = 4 \text{ k}\Omega$

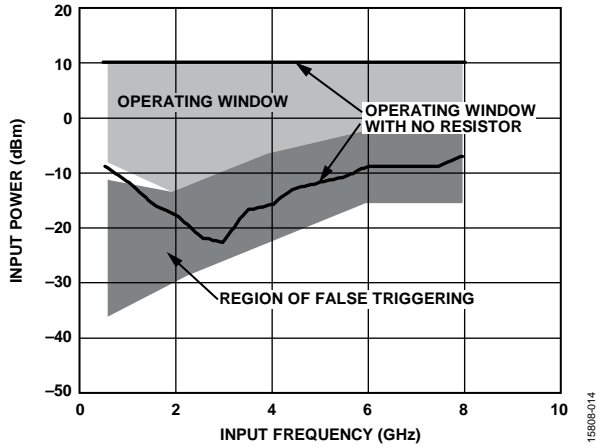


Figure 14. HMC434 Input Sensitivity and Operation, R5 = 4 kΩ

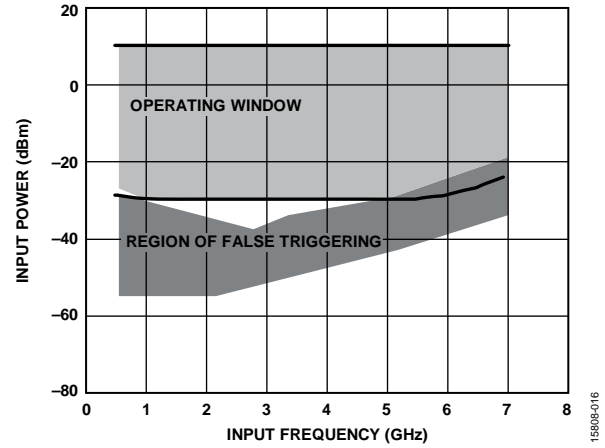


Figure 16. HMC438 Input Sensitivity and Operation, R5 = None

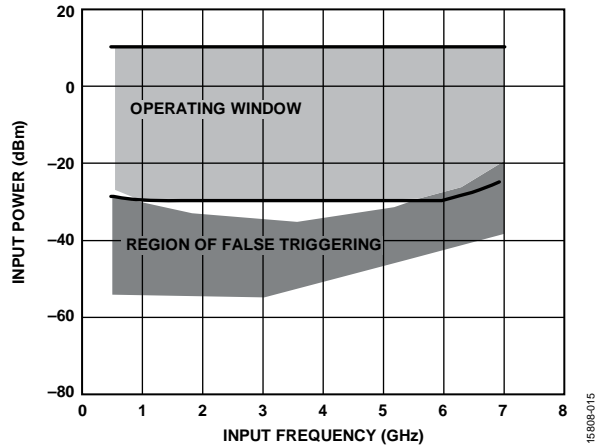


Figure 15. HMC437 Input Sensitivity and Operation, R5 = None