ANALOG DEVICES

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APPLICATION NOTE

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AD9786/AD9726 Calibration Engine

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INTRODUCTION

The AD9786 is a 16-bit, 500 MSPS CMOS DAC with selectable interpolation filters and a wide variety of signal processing features, making it ideal for many communications applications. The AD9786 calibration engine gives the user the flexibility to modify the factory calibration coefficients and to maintain the precise 16-bit linearity of the part in the presence of temperature fluctuations or other extraneous environmental conditions. The identical DAC core, calibration engine, and SPI® interface are also used in the AD9726, which is a 16-bit, 400 MSPS LVDS DAC, so this application note is applicable to both parts.

The AD9786 consists of a PMOS current source array capable of providing up to 20 mA of full-scale output current. This array is divided as follows:

- 127 equal current sources make up the 7 most significant bits (MSBs).
- The next 4 bits, or intermediate significant bits (ISBs), consist of 15 equal current sources which equal 1/16th of an MSB current
- The bottom 5 bits, or least significant bits (LSBs), consist of 5 binary weighted current sources that are fractions of the ISB current sources.

A factory calibration of the AD9786 improves the matching between the MSB segments along with the carry error between the sum of the ISBs and LSBs to one MSB segment. This procedure optimizes the linearity to achieve true 16-bit linear DC performance using internal calibration DACs. These calibration DACs utilize a volatile static memory word (SMEM) to determine how much current is added or subtracted from each segment. A factory calibration is stored in factory memory (FMEM) and on power up this memory is transferred to a static memory (SMEM) array. The SMEM can be modified via the serial port interface (SPI) through an internal self calibration, through a process that sets the static memory for each segment back to the default value (UNCAL), or by accessing and modifying the static memory of the individual segments. This application note explains how to perform these procedures, emphasizing the need for this capability in maintaining true 16-bit linearity over the entire operating temperature range.

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REVISION HISTORY

2/06—Revision 0: Initial Version

CALIBRATION DACS

The AD9786 has 128, 6-bit, calibration DACs used to calibrate the linearity performance. The DACs match the 127 MSB segments and match the sum of the ISB and LSB segments to that of an MSB segment. Each calibration DAC has a full scale of approximately 16 LSBs of the main DAC; thus 1 LSB of a calibration DAC equals 1/4th of an LSB of the main DAC. Figure 1 shows the typical gain curves for all 128 calibration DACs.

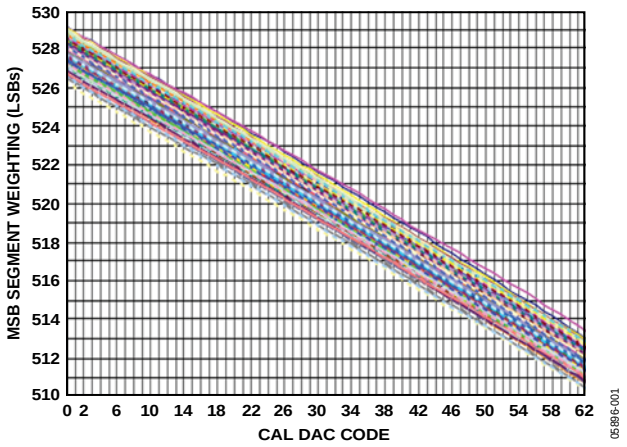

Figure 1. Typical Gain Curves for all 128 Linearity Calibration DACs

In addition to the 128 calibration DACs used to calibrate the linearity performance, there are another 4 calibration DACs used to calibrate the full-scale gain. During the factory calibration, the measured full-scale gain is adjusted to match the ideal full-scale gain more closely. Each gain calibration DAC has a full scale of approximately 520 LSBs of gain trim range, making 1 LSB of a calibration DAC equal to 8 LSBs of the main DAC. The measured coefficient for calibrating the gain either can be evenly distributed among the four gain calibration DACs or applied to one gain DAC, as the overall adjustment is through the sum of the four gain calibration DACs. Figure 2 shows the typical gain curves for the four gain calibration DACs.

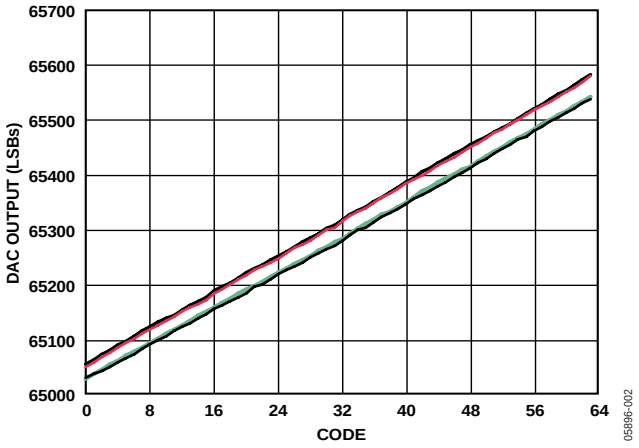

Figure 2. Typical Gain Curves for all 4 Full-Scale Gain Calibration DACs

As stated in the introduction, each calibration DAC is controlled via a volatile SMEM word, which is accessible through the SPI and is initiated to the factory memory (FMEM) at power up. The specific SPI registers necessary to access the SMEM are shown in Table 2.

Via the SPI, the user can modify the SMEM by accessing an individual calibration DAC to check the value currently in the SMEM, to modify the current value, or to uncalibrate the part. The next sections detail how to perform each of these functions.

CALMEMCK REGISTER

As shown in Table 1, the CALMEM bits in Register x0E indicate the state of the calibration memory at any time.

Table 1. CALMEM Bits in Register 0x0E

CALMEM [1]	CALMEM [0]	Calibration Memory State
0	0	Uncalibrated
0	1	Self-Calibrated
1	0	Factory-Calibrated
1	1	User Input

After performing a calibration, check the state of the CALMEM bits to ensure the operation was successful.

POWER-UP SEQUENCE

When the AD9786 is powered up, the factory calibration coefficients (FMEM) are transferred to the SMEM via an internal calibration clock (CALCK). The speed of the CALCK is a factor of the DAC clock rate and is determined by Register 0E Bits [2:0] as follows:

000: /32
001: /64
:
110: /2048
111: /4096

The default CALCK divider setting is 000, so that at power up the CALCK runs at FDAC/32. For reliable transfer from the FMEM to the SMEM, the CALCK should run at 10 MHz or below. So, for FDAC speeds above 320 MSPS, it is recommended to run a transfer enable (XFEREN) following a reset of the part with a larger CALCK divide ratio to ensure that the coefficients have transferred to the SMEM properly. The XFEREN function manually transfers the FMEM to the SMEM at the specified CALCK speed.

Note that the default CALCK divider setting for the AD9726 is /4096, so by default the CALCK is running at the slowest possible speed. For this reason, it should not be necessary to perform a transfer enable on the AD9726 at any operating speed.

Transfer Enable

To perform a transfer enable, follow these steps:

1. Reset the part.
2. Set CALCKDIV to /4096 (Register x0E, Bits [2:0] to x07).
3. Set XFEREN Bit high (Register x0F, Bit 4).
4. Perform an SPI write.
5. Set XFEREN bit low.
6. Perform an SPI write.
7. Read back the state of XFERSTAT bit (Register x0F, Bit 5). If this bit is high, the FMEM transfer to the SMEM is complete.

CALMEM should read back 10.

ACCESSING THE MEMORY

Each calibration DAC has a specified address assigned to it in order to access the SMEM or FMEM associated with it. As stated previously, there are 128 calibration DACs. To access a DAC, write one of these addresses into SPI Register x10:

MSB Segment 1 – MEMADDR 1
MSB Segment 2 – MEMADDR 2
:
MSB Segment 127 – MEMADDR 127
ISB/LSB Sum – MEMADDR 128
FSGAIN DAC 1 – MEMADDR 129
FSGAIN DAC 2 – MEMADDR 130
FSGAIN DAC 3 – MEMADDR 131
FSGAIN DAC 4 – MEMADDR 132

The user has both write and read access to the SMEM, but the FMEM is read only.

Read Access

To read from the SMEM or FMEM, follow these steps:

1. Set the address for the SMEM or FMEM location to be read from (Register x10).
2. If reading from SMEMEM, set SMEMRD (Register x0F, Bit 2). If reading from the FMEM set FMEMRD high (Register x0F, Bit 1).
3. Read back Register x11. This value corresponds to the volatile memory word for that specific calibration DAC.
4. Set SMEMRD low.
5. Repeat Step 1 to Step 4 to access multiple SMEM locations.

The CALMEM registers should not change state when performing a read back.

Write Access

To write to a specific calibration DAC, follow these steps:

1. Set address for the SMEM location to be written to (Register x10).
2. Set Register x11 to the value for writing to the memory location (maximum 63)
3. Set SMEMWR high (Register x0F, Bit 3).
4. Set SMEMWR low.
5. Repeat Step 1 to Step 4 to access multiple SMEM locations. The CALMEM should read back 11.

To access multiple SMEM locations for reading or writing, enter and exit the read or write functions before applying the address and data for the next location. Errors can occur if the SMEMRD or SMEMWR bits are set and all of the registers are read back or written to at one time. If the user externally modifies any of the SMEM coefficients, these coefficients are only valid until the part is reset or powered down, when the SMEM reverts to the factory-calibrated coefficients.

Table 2. SPI Registers to Access Calibration Engine

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALMEMCK	0E			CALMEM [1]	CALMEN [0]		CALCKDIV [2]	CALCKDIV [2]	CALCKDIV [2]
MEMRDWR	0F	CALSTAT	CALEN	XFERSTAT	XFEREN	SMEMWR	SMEMRD	FMEMRD	UNCAL
MEMADDR	10	MEMADDR [7]	MEMADDR [6]	MEMADDR [5]	MEMADDR [4]	MEMADDR [3]	MEMADDR [2]	MEMADDR [1]	MEMADDR [0]
MEMDATA	11			MEMDATA [5]	MEMDATA [4]	MEMDATA [3]	MEMDATA [2]	MEMDATA [1]	MEMDATA [0]

SELF-CALIBRATION

The factory calibration is performed at room temperature with an algorithm, optimizing both INL and DNL. To maintain the true 16-bit performance of the factory calibration, a self-calibration can be performed to help offset any linearity drift due to temperature. Note, however, that the self-calibration only optimizes DNL. The internal calibration engine selects a reference current, disconnects a segment from the output and adjusts the calibration DACs until the segment current equals the reference current; the segment current is then reconnected to the output and the current of another segment is calibrated. Because each segment's current is removed from the output during calibration, it cannot be used to generate data; the self-calibration should not be used while processing data. As with XFEREN, to ensure that the self-calibration is done successfully at speeds above 320 MSPS, CALCLKDIV must be set to the highest divider setting.

Performing a Self-Calibration

To perform a self-calibration, follow these steps:

1. Set CALCKDIV to /4096 (Register x0E, Bits [0:2] high).
2. Set CALEN Bit high (Register 0F, Bit 6).
3. Perform a SPI write.
4. Set CALEN bit low.
5. Do an SPI write and read at this point CALSTAT should now be high (Register 0F, Bit 7) meaning that the self-calibration is finished.

The CALMEM should now read back 01.

The following figures show the importance of the self-calibration function in maintaining 16-bit DNL performance. Figure 3 shows the factory-calibrated linearity with an INL spread of 1.6 LSBs and a DNL spread of ±0.4 LSBs. As shown in Figure 4, after soaking the part for 10 minutes at 85°C, the INL spread is approximately 6.5 LSBs and the DNL errors are as much as 1 LSB. In Figure 5, a self-calibration was then performed on the part at 85°C, which calibrated the INL back to a spread of approximately 2.5 LSBs with a maximum DNL error of −0.4 LSBs. The part was then soaked for 10 minutes at −40°C, as shown in Figure 6, degrading the INL performance to a spread of approximately 11 LSBs and maximum DNL errors of approximately 1.75 LSBs. In Figure 7, a self-calibration was once again performed on the part at −40°C. Again, the maximum DNL errors are approximately 0.4 LSBs and the INL spread is approximately 4 LSBs.

As seen in Figure 3 through Figure 7, performing a self-calibration at the temperature extremes allows the part to maintain the 16-bit DNL performance over the entire operating temperature range. There is a slight degradation in the INL performance because the self-calibration only calibrates out DNL errors in the part, without applying corrections to improve the INL performance.

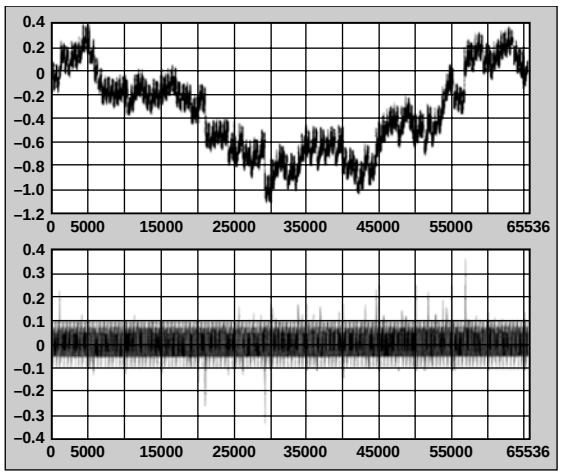

Figure 3. Post-Factory Calibration Linearity at 25°C (Top = INL, Bottom = DNL)

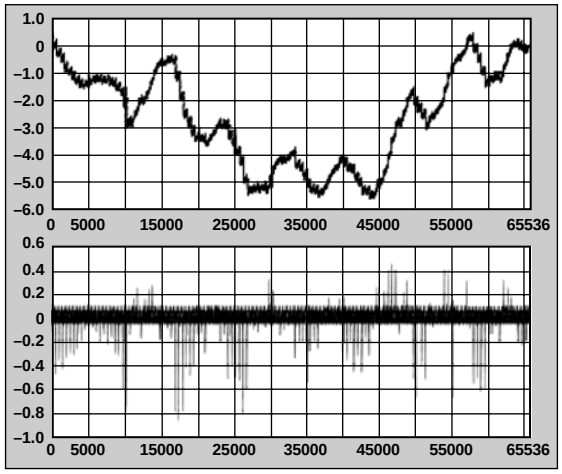

Figure 4. Linearity After 10-Minute Soak at 85°C (Top = INL, Bottom = DNL)

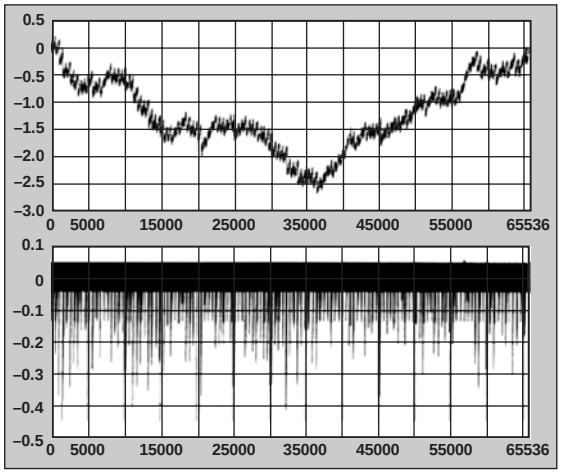

Figure 5. Post-Self-Calibration Linearity at 85°C (Top = INL, Bottom = DNL)

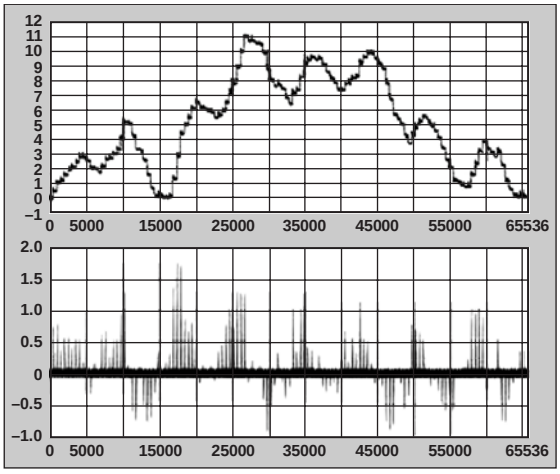

Figure 6 .Linearity After 10 Minute Soak at –40°C (Top = INL, Bottom = DNL)

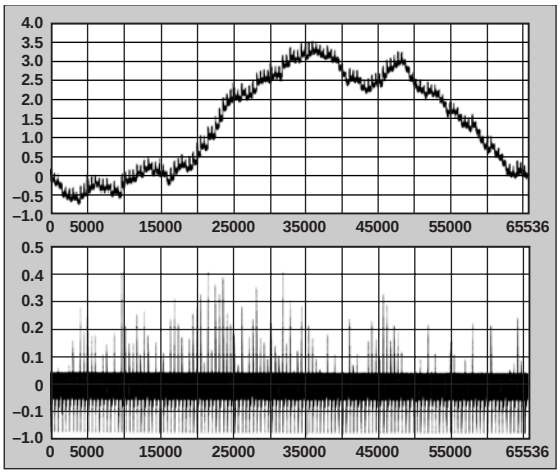

Figure 7. Post Self-Calibration Linearity at –40°C (Top = INL, Bottom = DNL)

USING THE AD9786 IN AN UNCALIBRATED STATE

Additionally, users can completely uncalibrate the part and return the SMEM to its default state with a coefficient of 63 in all SMEM locations. However, this is not recommended in cases where the AD9786 must maintain precise linearity.

Uncalibrating the AD9786

To uncalibrate the part, follow these steps:

1. Set CALCKDIV to /4096 (Register x0E, Bits [0:2] high).
2. Set UNCAL bit high (Register x0F, Bit 0).

As with the self-calibration, there is a change in state of Register x0E Bits [5:4]. These bits read back as a 00, indicating that the part has been uncalibrated. The CALMEM should read back 00.

CONCLUSION

The AD9786 calibration engine gives the user the flexibility to modify the factory calibration coefficients, if desired, in order to maintain the precise 16-bit linearity of the part in the presence of temperature fluctuations or other extraneous environmental conditions.

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