AD602JRZ

SP Amp Variable Gain Amp Dual ±5.25V 16-Pin SOIC W Tube

Manufacturer:	Analog Devices, Inc
Package/Case:	SOP16
Product Type:	Amplifier ICs
RoHS:	RoHS Compliant/Lead free
Lifecycle:	Active

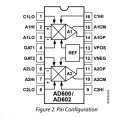


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	C1LO	CH1 Gain-Control Input Low. Positive voltage reduces CH1 gain.
2	A1HI	CH1 Signal Input High. Positive voltage increases CH1 output.
3	A1LO	CH1 Signal Input Low. Usually connected to CH1 input ground.
4	GAT1	CH1 Gating Input. A logic high shuts off the CH1 signal path.
5	GAT2	CH2 Gating Input. A logic high shuts off the CH2 signal path.
6	A2LO	CH2 Signal Input Low. Usually connected to CH2 input ground.
7	A2HI	CH2 Signal Input High. Positive voltage increases CH2 output.
8	C2LO	CH2 Gain-Control Input Low. Positive voltage reduces CH2 gain.
9	C2HI	CH2 Gain-Control Input High. Positive voltage increases CH2 gain.
10	A2CM	CH2 Common. Usually connected to CH2 output ground.
11	A2OP	CH2 Output.
12	VNEG	Negative Supply for Both Amplifiers.
13	VPOS	Positive Supply for Both Amplifiers.
14	A1OP	CH1 Output.
15	A1CM	CH1 Common. Usually connected to CH1 output ground.
16	C1HI	CH1 Gain-Control Input High. Positive voltage increases CH1 gain.

Images are for reference only

Inquiry

General Description

The AD600/AD602 dual channel, low noise, variable gain amplifiers are optimized for use in ultrasound imaging systems, but are applicable to any application requiring precise gain, low noise and distortion, and wide bandwidth. Each independent channel provides a gain of 0 dB to +40 dB in the AD600 and –10 dB to +30 dB in the AD602. The lower gain of the AD602 results in an improved signal-to-noise ratio (SNR) at the output. However, both products have the same 1.4 nV/√Hz input noise spectral density. The decibel gain is directly proportional to the control voltage, accurately calibrated, and supply and temperature-stable.

To achieve the difficult performance objectives, a proprietary circuit form, the X-AMP®, was developed. Each channel of the X-AMP comprises a variable attenuator of 0 dB to –42.14 dB followed by a high speed fixed gain amplifier. In this way, the amplifier never has to cope with large inputs, and can benefit from the use of negative feedback to precisely define the gain and dynamics. The attenuator is realized as a 7-stage R-2R ladder network having an input resistance of 100 W, laser trimmed to ±2%. The attenuation between tap points is 6.02 dB; the gain-control circuit provides continuous interpolation between these taps. The resulting control function is linear in dB.

The gain-control interfaces are fully differential, providing an input resistance of ~15 M W and a scale factor of 32 dB/V (that is, 31.25 mV/dB) defined by an internal voltage reference. The response time of this interface is less than 1 µs. Each channel also has an independent gating facility that optionally blocks signal transmission and sets the dc output level to within a few millivolts of the output ground. The gating control input is TTL- and CMOS-compatible.

The maximum gain of the AD600 is 41.07 dB, and the maximum gain of the AD602 is 31.07 dB; the –3 dB bandwidth of both models is nominally 35 MHz, essentially independent of the gain. The SNR for a 1 V rms output and a 1 MHz noise bandwidth is typically 76 dB for the AD600 and 86 dB for the AD602. The amplitude response is flat within ±0.5 dB from 100 kHz to 10 MHz; over this frequency range, the group delay varies by less than ±2 ns at all gain settings.

Each amplifier channel can drive 100 W load impedances with low distortion. For example, the peak specified output is ±2.5 V minimum into a 500 W load, or ±1 V into a 100 W load. For a 200 W load in shunt with 5 pF, the total harmonic distortion for a ±1 V sinusoidal output at 10 MHz is typically -60 dBc.

The AD600J/AD602J are specified for operation from 0°C to 70°C and are available in 16-lead PDIP (N) and 16-lead SOIC packages. The AD600A/AD602A are specified for operation from –40°C to +85°C and are available in 16-lead CERDIP (Q) and 16-lead SOIC packages.The AD600S/AD602S are specified for operation from –55°C to +125°C, are available in a 16-lead CERDIP (Q) package, and are MIL-STD-883 compliant. The AD600S/AD602S are also available under DESC SMD 5962-94572.

AD600 - Gain Range:0 dB to 40 dB

AD602 - Gain Range:–10 dB to + 30 dB

Key Features

2 channels with independent gain control Linear in dB gain response

2 gain ranges AD600: 0 dB to 40 dBAD602: -10 dB to +30 dB

Accurate absolute gain: ±0.3 dB

Low input noise: 1.4 nV/√Hz

Low distortion: -60 dBc THD at ±1 V output

High bandwidth: dc to 35 MHz (-3 dB)

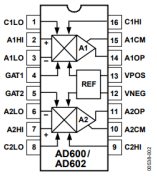
Stable group delay: ±2 ns

Low power: 125 mW (maximum) per amplifier

Signal gating function for each amplifier

Drives high speed ADCs

MIL-STD-883-compliant and DESC versions available



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5	GAT2	CH2 Gating Input. A logic high shuts off the CH2 signal path.
6	A2LO	CH2 Signal Input Low. Usually connected to CH2 input ground.
7	A2HI	CH2 Signal Input High. Positive voltage increases CH2 output.
8	C2LO	CH2 Gain-Control Input Low. Positive voltage reduces CH2 gain.
9	C2HI	CH2 Gain-Control Input High. Positive voltage increases CH2 gain.
10	A2CM	CH2 Common. Usually connected to CH2 output ground.
11	A2OP	CH2 Output.
12	VNEG	Negative Supply for Both Amplifiers.
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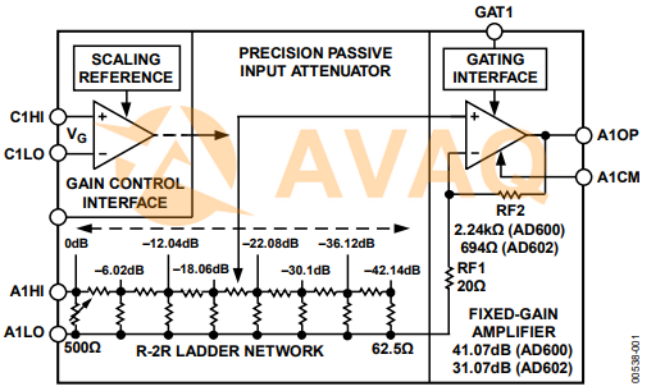
FUNCTIONAL BLOCK DIAGRAM



Recommended For You

AD8309ARUZ

Analog Devices, Inc

TSSOP16

AD524BDZ

Analog Devices, Inc

CDIP-16

AD8221BR

Analog Devices, Inc

SOP-8

AD8221ARZ

Analog Devices, Inc

SOP8

AD627BRZ

Analog Devices, Inc

SOP8

AD622ANZ

Analog Devices, Inc

DIP8

ADA4930-2YCPZ-R7

Analog Devices, Inc

LFCSP24

AD8034ARZ

Analog Devices, Inc

SOP8

AD8561ARZ

Analog Devices, Inc

SOP8

AD633JRZ

Analog Devices, Inc

SOP8

AD632AH

Analog Devices, Inc

CAN10

AD8422BRZ

Analog Devices, Inc

SOP8

ADCMP600BKSZ-R2

Analog Devices, Inc

SC70-5

AD620BN

Analog Devices, Inc

DIP8

AD620BR

Analog Devices, Inc

SOP